FM8PC75AM

FTC 8-Bits Micro-Controller With 12-Bits ADC & Comparator

Datasheet E0.1
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Version Control

Version	Date	Description
E01	2021-02-05	Release of prototype

Contents

【1】 FM8PC75AM Review

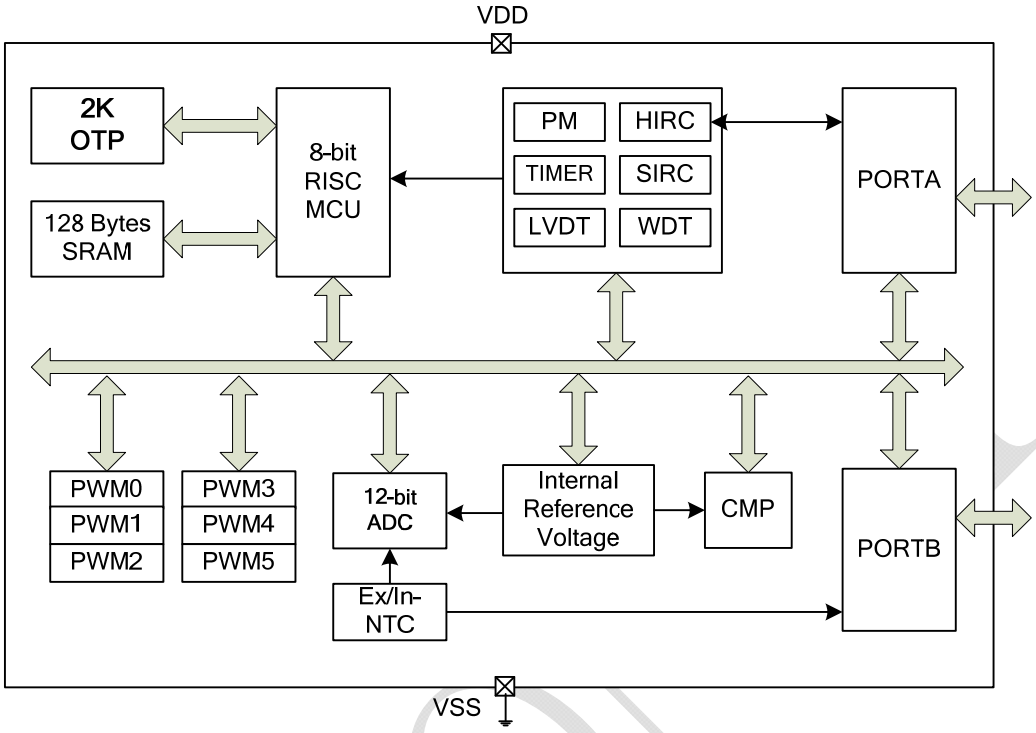
1.1 Description

FM8PC75AM is an EPROM based 8-bit MCU. FM8PC75AM adopts CMOS technology to provide 8(6+2) channel 12-bit ADC (VREFHmin=1V), six 8-bit PWM (or three 16- bitPWM), one hardware comparator, one 16-bit and two 8-bit counters, internal and external temperature sensing detect (NTC). FM8PC75AM built in high precision internal high-frequency clock (HIRC), voltage detector and low-frequency clock (SIRC).

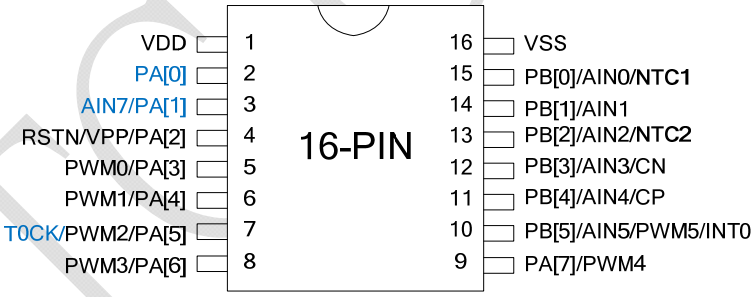
1.2 Feature

- **8-bit RISC microprocessor**
  - 2 CPU clock per instruction (2T), except branch instruction.
  - 2 K OTP.
  - 8 level stack
  - 128 bytes SRAM.
  - High Speed Internal clock, 16Mhz/8Mhz is according by writer's configuration.
  - One 16-bit and two 8-bit counters.
  - Watch dog timer.
- **System Clock**
  - Internal Oscillator
    - 16MHz/8Mhz oscillator (writer select option)
    - 32KHz oscillator
- **14 I/O ports**
  - General IO provide normal driving capacity
  - PA[7], PA[6], PA[4], PA[2], PB[6] provide enhance driving capacity.
  - PA[5], PA[3], provide highest driving capacity.
  - Each IO pin provides high-impedance input, internal pull-high, open drain output or CMOS output.
  - Each IO pin can wake-up MCU. .
  - PB[3]、PB[4] can be wire-and..
- **1+10 Interrupt sources**
  - One external interrupt source: INT0(PB[5]).
  - Ten internal interrupt sources: Timer1, LVDT, CMP, ADC, PWM5~0
- **6+2 Channel 12bit ADC**
  - Optional Continues or Trigger mode to sample
  - Supports 6 channel external ADC input (include 2 NTC channel) , an internal reference and internal NTC.
  - Build in AD reference voltage (**VDD, 4V, 3V, 2V,1.2V, 1V**).
- **Power Manager**
  - Power on reset 2.4V(POR)
  - Power down reset 2.35V(PDR)
  - 4-level voltage detect: 4.3V, 3.6V, 3.0V, 2.7V.
- **PWM Function**
  - Supports 8bit PWM*6 or 16bit PWM*3 (maximum frequency 16Mhz)
  - Change PWM output by program.
- **Temperature Sensing Detect**
  - One internal temperature sensing detect(INTC), Two external constant-current temperature sensing detect(NTC1,NTC2)
- **Comparator**
  - Sixteen level reference voltage.
  - Build in reference voltage (1.0V).

1.3 Block Diagram



1.4 Pin Definitions



FM8PC75AM
DIP/SOP16

1.5 Pin Description

PIN Name	I/O	14-pin P	16-pin S	Description
VDD	I	1	1	Power
PA[0]	IO	2	2	Bidirectional I/O pin. Provide pull-high or high-impedance input.
PA[1]	IO	3	3	Bidirectional I/O pin. Provide pull-high or high-impedance input.
PA[2] VPP RSTN	I I I	4	4	Bidirectional I/O pin (Open Drain). **Note: Do not exceed Vdd.** Provide pull-high or high-impedance input. (Open Drain). Programming Pin External reset (low voltage active).
PA[3] PWM0	IO O	5	5	Bidirectional I/O pin (Open Drain). Provide pull-high or high-impedance input. PWM0 output
PA[4] PWM1	IO O	6	6	Bidirectional I/O pin (Open Drain). Provide pull-high or high-impedance input. PWM1 output
PA[5] PWM2 T0CK	IO I I	7	7	Bidirectional I/O pin (Open Drain). Provide pull-high or high-impedance input. PWM2 output Tiimer0 external clock input
PA[6] PWM3	IO O	--	8	Bidirectional I/O pin (Open Drain). Provide pull-high or high-impedance input. PWM3 output
PA[7] PWM4	IO O	--	9	Bidirectional I/O pin (Open Drain). Provide pull-high or high-impedance input. PWM4 output
PB[5] INT0 PWM5	IO I O	8	10	Bidirectional I/O pin (Open Drain). Provide pull-high or high-impedance input. Wake up pin External interrupt pin PWM5 output

PIN Name	I/O	14-pin P	16-pin S	Description
PB[4]	IO	9	11	Bidirectional I/O pin (Open Drain). Provide pull-high or high-impedance input. Wake up pin
AIN4	I			ADC input channel 4
CP	I			Positive comparator input.
PB[3]	IO	10	12	Bidirectional I/O pin (Open Drain). Provide pull-high or high-impedance input. Wake up pin
AIN3	I			ADC input channel 3
CN	I			Negative comparator input.
PB[2]	IO	11	13	Bidirectional I/O pin (Open Drain). Provide pull-high or high-impedance input. Wake up pin
AIN2	I			ADC input channel 2
NTC2	A			Constant current output 2.
PB[1]	IO	12	14	Bidirectional I/O pin (Open Drain). Provide pull-high or high-impedance input. Wake up pin
AIN1	I			ADC input channel 1
PB[0]	IO	13	15	Bidirectional I/O pin (Open Drain). Provide pull-high or high-impedance input. Wake up pin
AIN0	I			ADC input channel 0
NTC1	A			Constant current output 1.
VSS	G	14	16	Ground

1.6 Brief Pin Function

Pin Name	*Voltage*	*8B-PWM*	*16B-PWM Same/complement Output*	*NTC*	*ADC*	*CMP/ Ex-Interrupt/ T0CK*	*Short*	*Write PIN*
VDD	P							V
PA[0]	**I/O**							
PA[1]	**I/O**				AIN7			V
PA[2]	**I/O(VPP)**							V
PA[3]	**I/O**	PWM0	PWM01H					
PA[4]	**I/O**	PWM1	PWM01L					
PA[5]	**I/O**	PWM2	PWM23H			T0CK		
PA[6]	**I/O**	PWM3	PWM23L					
PA[7]	**I/O**	PWM4	PWM45					
PB[5]	**I/O**	PWM5			AIN5	INT0		
PB[4]	**I/O**				AIN4	CP	V	
PB[3]	**I/O**				AIN3	CN	V	
PB[2]	**I/O**			NTC2	AIN2			
PB[1]	**I/O**				AIN1			V
PB[0]	**I/O**			NTC1	AIN0			V
VSS	**G**							V

【2】 Absolute Maximum Ratings

Parameter	Conditions	Value		Unit
		Min	Max	
Ambient Operating Temperature	-	-40	70	℃
Storage Temperature	-	-40	150	℃
DC Supply Voltage	-Respect to VSS	2.0	5.5	V
Supply Current	-	-	-	mA
Voltage on all GPIO pin	Respect to VSS	-0.3	VDD+0.3V	V

【3】 Electrical Characteristics

3.1 DC Characteristics (Operating Temperature = 0 to 70 ℃)

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
VDD	Operating Voltage	--	2.4	5.0	5.5	V
LVR	LVR Accuracy		-5%		5%	%
I_{dd1}	Normal Mode Operating Current Typical = (Disable ADC)	Vdd=5V,No GPIO loading IRC Operating , FCPU=16MHz	1.8	2.0	2.2	mA
	Normal Mode Operating Current Typical = (Disable ADC)	Vdd=3V,No GPIO loading IRC Operating , FCPU=16MHz	0.8	1.0	1.2	mA
	Normal Mode Operating Current Typical = (Disable ADC)	Vdd=5V,No GPIO loading IRC Operating , FCPU=8MHz	1.0	1.2	1.4	mA
	Normal Mode Operating Current Typical = (Disable ADC)	Vdd=3V,No GPIO loading IRC Operating , FCPU=8MHz	0.40	0.55	0.70	mA
I_{dd2}	Slow Mode Operating Current Typical = (Disable ADC)	Vdd=5V,No GPIO loading SIRC Operating, FCPU=32KHz	650	800	950	uA
	Slow Mode Operating Current Typical = (Disable ADC)	Vdd=3V,No GPIO loading SIRC Operating, FCPU=16KHz	250	350	500	uA
I_{dd3}	Green Mode Operating Current (watch Dog Enable) Typical = (Disable ADC /LVDT)	Vdd=5V, No GPIO loading WDT = 32ms ,FCPU=Disable	7	10	15	uA
I_{dd4}	Green Mode Operating Current (watch Dog Disable) Typical = (Disable ADC /LVDT)	Vdd=5V,No GPIO loading @25 ℃	2	2.5	5	uA
	Green Mode Operating Current (watch Dog Disable) Typical = (Disable ADC /LVDT)	Vdd=3V,No GPIO loading @25 ℃	0.5	1	2	uA
V_{LVDT}	Low Voltage Detect (LVDT43, LVDT36,LVDT30, LVDT27)		-5%		5%	%
V_{POR}	Power Reset	Power 0V to VDD (VIH) (POR)		2.4		V
		Power VDD to 0V (VIL) (PDR)		2.35		V
F_{CPU}	MCU work frequency	25 ℃, VDD > 2.5V			8	MHz
		25 ℃, VDD > 3.0V			16	MHz

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
F_{IRC}	Internal high RC frequency	VDD=5V, 25 ℃, F_{IRC}16Mhz △ = 16 * (2%)	16 - △	16	16+△	MHz
		VDD=3~5V, @25℃ F_{IRC} = 16Mhz △ = 16 * (2%)	16 - △	16	16+△	MHz
		VDD=5V, 25 ℃, F_{IRC}8Mhz △ = 16 * (2%)	8 - △	8	8+△	MHz
		VDD=2.4~5V, @25℃ F_{IRC} = 8Mhz △ = 16 * (2%)	8 - △	8	8+△	MHz
F_{SIRC}	Internal slow RC frequency	VDD=2.2~5V, @25℃ △ = 32 * (10 %)	32 -△	32	32+△	KHz
T_{POREXT}	Power on reset Timing	VDD =5V	1.3	2	3	mS
		VDD =3V	1.4	2	3	mS

3.2 IO Characteristics

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
V_{up1}	GPIO Pull-up Resistor	VDD=5V	70	100	130	KΩ
V_{up2}	GPIO Pull-up Resistor	VDD=3V	70	100	130	KΩ
I_{OL1}	Sink Current PA[3],PA[5]	VDD=5V, V_{OL}=0.5		40		mA
I_{OL2}	Sink Current PA[2],PA[4],PA[6], PA[7],PB[6]	VDD=5V, V_{OL}=0.5		20		mA
I_{OL3}	Sink Current PA[0],PA[1]PB[5],PB[4], PB[3],PB[2],PB[1],PB[0]	VDD=5V, V_{OL}=0.5		15		mA
I_{OH1}	Drive Current PA[3],PA[5]	VDD=5V, V_{OH}=4.5		20		mA
I_{OH2}	Drive Current PA[2],PA[4],PA[6], PA[7],PB[6] PA[0],PA[1]PB[5],PB[4], PB[3],PB[2],PB[1],PB[0]	VDD=5V, V_{OH}=4.5		6.5		mA
V_{IL1}	Input Low Voltage	VDD=2.4~5.5V	0		0.3*VDD	V
V_{IH1}	Input High Voltage	VDD=2.4~5.5V	0.7*VDD		VDD	V
V_{IL2}	Input Low Voltage PA[2]	VDD=2.4~5.5V	0		0.2*VDD	
V_{IH2}	Input High Voltage PA[2]	VDD=2.4~5.5V	0.5*VDD		VDD	
I_{NTC}	Current source PB[0],PB[2]	VDD=3~5V, @25℃ Enable NTC0 ,NTC1 PB[0] ,PB[2	70	100	130	uA

3.3 ADC specification

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
ADCSR	ADC sample Rate	FADC = ADC clock		14		FADC
DNL	Differential Nonlinearity	Resolution = 12bit VDD=5.0V, VREFH = 3V FADCSR=32K		2		LSB
INL	Integral Nonlinearity	Resolution = 12bit VDD=5.0V, VREFH = 3V FADCSR=32K		2		LSB
GE	Gain Error	Resolution = 12bit VDD=5.0V, VREFH = 3V FADCSR=32K		1	--	LSB
VINREFH	ADC Internal Reference Voltage	VINREFH = 4V (Vdd=5V~4.4V, -20~85℃) △ = 4V * (2%)	4-△	4	4+△	V
		VINREFH = 3V (Vdd=5V~3.3V, -20~85℃) △ = 3V * (2%)	3-△	3	3+△	V
		VINREFH = 2V (Vdd=5V~2.6V, -20~85℃) △ = 2V * (2%)	2-△	2	2+△	V
		VINREFH = 1V (Vdd=5V~2.4V, -20~85℃) △ = 1V * (2%)	1-△	1	1+△	V

3.4 CMP specification

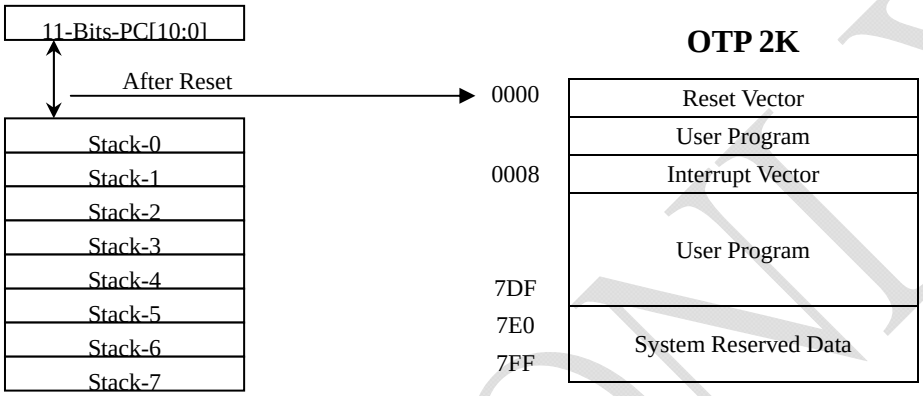
Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
VIO	Input offset voltage	VDD=5V~2.0V		+/-15	+/-40	mV
VICM	Input common mode voltage	VDD=5V~2.0V	0.02		VDD-1	V
TSTB	Stable time	@VDD=5V, 25℃		150	300	ns
VREFH	Internal Reference Voltage	@VDD=5V, 25℃	0.95	1	1.05	V

【4】 Function Decription

4.1 MCU Uuit

4.1-1 OTP Memory

The FM8PC75AM have a 11-bit Program Counter capable of addressing a 2K program memory space. It has described in the following table.



4.1-2 Control Register

Table 4.1-2.1 I/O and Control Register Mapping

Address	Description(F-plane)	Address	R-Plane
00h	INDF		
01h	PCHBUF		
02h	PCL		
03h	STATUS		
04h	FSR		
05h	IOSTA		
06h	PORTA		
07h	IOSTB		
08h	PORTB		
09h	T1CON		
0Ah	TMR1LB		
0Bh	TMR1HB		
0Ch	IRCWCON		
0Dh	LVDTCON		
0Eh	INTEN		
0Fh	INTFLAG		
10h	PWMEN	10h	PSEL
11h	PWMPADEN		
12h	PWM01CON		
13h	PWM23CON		
14h	PWM45CON		
15h	PWM0Duty		

Address	Description(F-plane)	Address	R-Plane
16h	PWM1Duty		
17h	PWM2Duty		
18h	PWM3Duty		
19h	PWM4Duty		
1Ah	PWM5Duty		
1Bh	PWM0PR		
1Ch	PWM1PR		
1Dh	PWM2PR		
1Eh	PWM3PR		
1Fh	PWM4PR		
20h	PWM5PR		
21h	TSDCON		
22h	CMPCON1		
23h	CMPCON2		
24h	PWMINTEN		
25h	PWMINTFLAG		
26h	AWUCON		
27h	APHCON		
28h	BWUCON		
29h	BPHCON		
2Ah	PWMOSL		
2Bh	ADCON1		
2Ch	ADCON2		
2Dh	ADCON3		
2Eh	ADCHB		
2Fh	ADCLB		
30 | 4Fh	32 Byte SRAM		
50h | 7Fh	RAMBK=0	RAMBK=1	
	SRAM 48bytes	SRAM 48bytes	

4.1-3 Control Register Definition

TABLE 4.1-3.1: Control Register Map

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
System									
0x00 (r/w)	INDF	Uses contents of FSR to address data memory (not a physical register)							
0x01(r/w)	PCHBUF	-	-	-	-	--	3 MSBs Buffer of PC		
0x02 (r/w)	PCL	Low order 8 bits of PC							
0x03 (r/w)	STATUS	RST	RESTORE	RAMBK	$\overline{TO}$	$\overline{PD}$	Z	DC	C
0x04 (r/w)	FSR	Indirect data memory address pointer							
0x05 (r/w)	IOSTA	IOSTA7	IOSTA6	IOSTA5	IOSTA4	IOSTA3	*IOSTA2	IOSTA1	IOSTA0
0x06 (r/w)	PORTA	IOA7	IOA6	IOA5	IOA4	IOA3	*IOA2	IOA1	IOA0
0x07 (r/w)	IOSTB	-	-	IOSTB5	IOSTB4	IOSTB3	IOSTB2	IOSTB1	IOSTB0
0x08 (r/w)	PORTB	-	-	IOB5	IOB4	IOB3	IOB2	IOB1	IOB0
0x09 (r/w)	T1CON	-	-	-	T1PS1	T1PS0	T1CS1	T1CS0	T1EN
0x0A (r/w)	TMR1LB	Low byte of 16-bit real-time clock/counter 1							
0x0B (r/w)	TMR1HB	High byte of 16-bit real-time clock/counter 1							
0x0C (r/w)	IRCWCON	WDTEN	HIRCEN	WS1	WS0	CPUS	IRCF2	IRCF1	IRCF0
0x0D (r/w)	LVDTCON	EIS	RDPORT	RA2EN	LVENB	INTEDG	SEN	S1	S0

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x0E (r/w)	INTEN	GIE	-	-	LVDTIE	CMPIE	INTIE	-	T1IE
0x0F (r/w)	INTFLAG	-	-	-	LVDTIF	CMPIF	INTIF	-	T1IF
0x10 (r/w)	PWMEN	P23EN	P01EN	P5EN	P4EN	P3EN	P2EN	P1EN	P0EN
0x11 (r/w)	PWMPADEN		P45EN	P5PADEN	P4PADEN	P3PADEN	P2PADEN	P1PADEN	P0PADEN
0x12 (r/w)	PWM01CON	P1CK1	P1CK0	P1Pole1	P1Pole0	P0CK1	P0CK0	P0Pole1	P0Pole0
0x13 (r/w)	PWM23CON	P3CK1	P3CK0	P3Pole1	P3Pole0	P2CK1	P2CK0	P2Pole1	P2Pole0
0x14 (r/w)	PWM45CON	P5CK1	P5CK0	P5Pole1	P5Pole0	P4CK1	P4CK0	P4Pole1	P4Pole0
0x15 (r/w)	PWM0Duty	P0D7	P0D6	P0D5	P0D4	P0D3	P0D2	P0D1	P0D0
0x16 (r/w)	PWM1Duty	P1D7	P1D6	P1D5	P1D4	P1D3	P1D2	P1D1	P1D0
0x17 (r/w)	PWM2Duty	P2D7	P2D6	P2D5	P2D4	P2D3	P2D2	P2D1	P2D0
0x18 (r/w)	PWM3Duty	P3D7	P3D6	P3D5	P3D4	P3D3	P3D2	P3D1	P3D0
0x19 (r/w)	PWM4Duty	P4D7	P4D6	P4D5	P4D4	P4D3	P4D2	P4D1	P4D0
0x1A (r/w)	PWM5Duty	P5D7	P5D6	P5D5	P5D4	P5D3	P5D2	P5D1	P5D0
0x1B (r/w)	PWM0PR	P0PR7	P0PR6	P0PR5	P0PR4	P0PR3	P0PR2	P0PR1	P0PR0
0x1C (r/w)	PWM1PR	P1PR7	P1PR6	P1PR5	P1PR4	P1PR3	P1PR2	P1PR1	P1PR0
0x1D (r/w)	PWM2PR	P2PR7	P2PR6	P2PR5	P2PR4	P2PR3	P2PR2	P2PR1	P2PR0
0x1E (r/w)	PWM3PR	P3PR7	P3PR6	P3PR5	P3PR4	P3PR3	P3PR2	P3PR1	P3PR0
0x1F (r/w)	PWM4PR	P4PR7	P4PR6	P4PR5	P4PR4	P4PR3	P4PR2	P4PR1	P4PR0
0x20 (r/w)	PWM5PR	P5PR7	P5PR6	P5PR5	P5PR4	P5PR3	P5PR2	P5PR1	P5PR0
0x21 (r/w)	TSDCON	NTC1EN	NTC2EN	TSDEN	DTSL2	DTSL1	DTSL0	VOTPSL[1:0]	
0x22 (r/w)	CMPCON1	LVDTSV(R)	-	COUT(R)	CINV	CINS	CM2	CM1	CM0
0x23 (r/w)	CMPCON2	CVREN	-	CVRR	-	CVR3	CVR2	CVR1	CVR0
0x24 (r/w)	PWMINTEN	-	-	P5IEN	P4IEN	P3IEN	P2IEN	P1IEN	P0IEN
0x25 (r/w)	PWMINTFLAG	-	-	P5IF	P4IF	P3IF	P2IF	P1IF	P0IF
0x26 (r/w)	AWUCON	AWE[7]	AWE[6]	AWE[5]	AWE[4]	AWE[3]	AWE[2]	AWE[1]	AWE[0]
0x27 (r/w)	APHCON	APH[7]	APH[6]	APH[5]	APH[4]	APH[3]	APH[2]	APH[1]	APH[0]
0x28 (r/w)	BWUCON	UGMD	GreenL	BWE[5]	BWE[4]	BWE[3]	BWE[2]	BWE[1]	BWE[0]
0x29 (r/w)	BPHCON	INEN_PA1	-	BPH[5]	BPH[4]	BPH[3]	BPH[2]	BPH[1]	BPH[0]
0x2A (r/w)	PWMOSL	P3SEL[1:0]		P2SEL[1:0]		P1SEL[1:0]		P0SEL[1:0]	
0x2B (r/w)	ADCON1	ADCEN	ADCST	CHSEL[2:0]			INSEL	ADCSR[1:0]	
0x2C (r/w)	ADCON2	ADCIE	ADCIF	SVREFH	ADCNT	ADCTMS	SELVER[2:0]		
0x2D (r/w)	ADCON3	CONCH[1:0]		INEN[5]	INEN[4]	INEN[3]	INEN[2]	INEN[1]	INEN[0]
0x2E (r)	ADCHB	ADCB[11:4]							
0x2F (r)	ADCLB	-	-	-	-	ADCB[3:0]			
IOST Area									
0x10	PSEL	-	-	PS5	PS4	PS3	PS2	PS1	PS0

Legend: - = unimplemented, read as '0'.
GP = General Purpose Bit
* = Open Drain output.

4.2 Clock Control

Frequency range : (Fcpu is MCU operating clock)
(1) When Power on, Fcpu = Fsirc (32KHz)
(2) When VDD > 2.4V → Fcpu ≦ 8Mhz

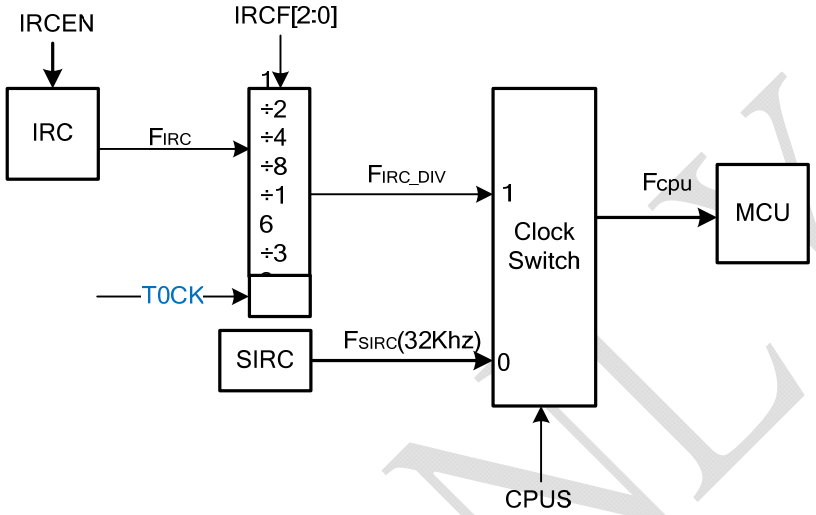


***Figure* 4.2-1 Clock Switching Diagram**

4.3 Counter

4.3-1 16bitCounter-1(Timer1)

Timer1 is a 16bit counter ,Timer1 clock source can be from FCPU, FIRC, Timer2 output and external pin (T0CK) . Timer1diagram as Figure 4.3-1.

(1) Timer1 initial count : 16'h0000→16'FFFF→16'F0000

(2) Timer1 TM1RLD reload count : {TM1HB,TM1LB} →16'FFFF→16'F0000

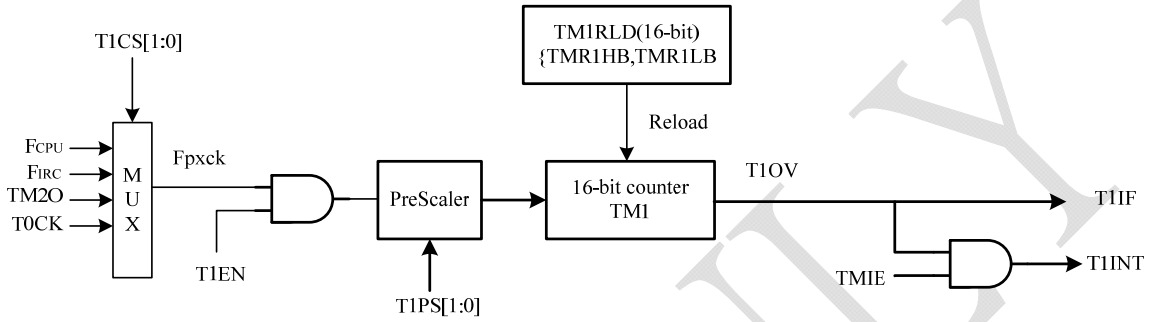


***Figure* 4.3-1Timer1 Diagram**

Timer1 clock source selection

{T1CS1,T1CS0}	Clock Source
2'b00	FCPU
2'b01	FIRC (16Mhz / 8Mhz)
2'b10	Timer2 output
2'b11	T0CK (External clock)

4.3-2 8bit Counter-2,3(Timer2,Timer3)

Timer2 (PWM4) and Timer3 (PWM5) are 8-bit counters.

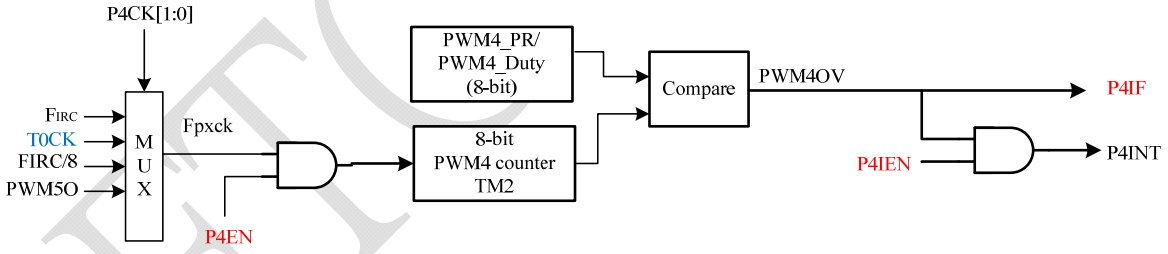


***Figure* 4.3-2.1 Timer2 Diagram**

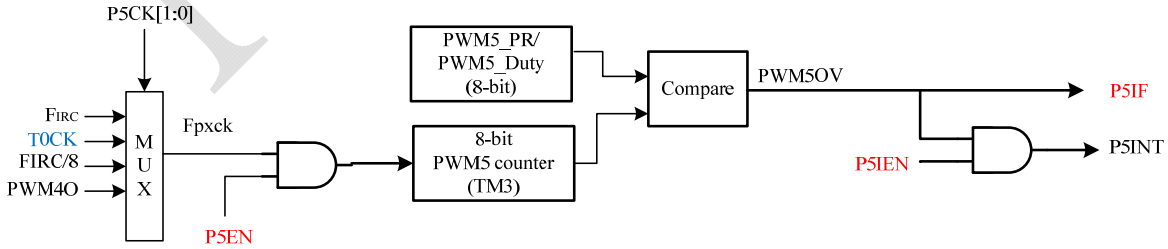


***Figure* 4.3-2.2 Timer3 Diagram**

4.3-3 Watchdog Timer (WDT)

The Watchdog Timer (WDT) is a free running on chip RC oscillator which dose not require any external components. So the WDT will still run into GREEN mode. During normal operation or in GREEN mode, a WDT time-out will cause base on Configuration option to the device reset .。

Configuration WS[1:0]	WDT Time out
2'b11	18 ms
2'b10	72 ms
2'b01	288 ms
2'b00	2S ms

表 4.3-3.1

The CLRWDT instruction clears the WDT, if assigned to the WDT, and prevents it from timing out and generating a device reset.
The WDT can be disabled by clearing the control bit WDTE(08h-7). The WDT has a normal time-out period of 18ms(without precaler). When the SLEEP instruction executes, the MCU will be reset when WDT time-out.
The prescaler of WDT refers **Table 4.3-3.1**
The block diagram of WDT shows in ***Figure* 4.3-3.2**.

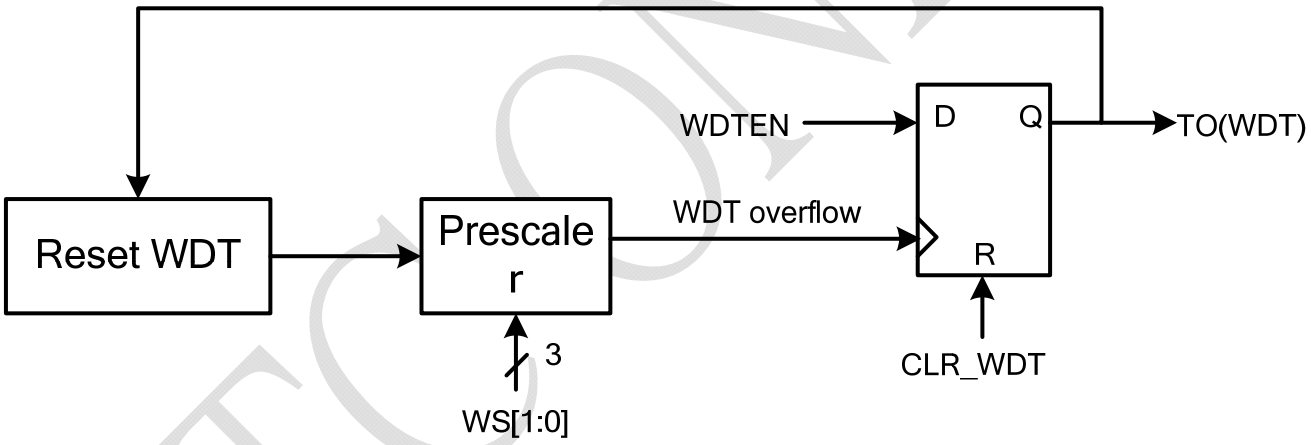


***Figure* 4.3-3.2 WDT Diagram**

4.4 Power and Reset Management

There are five cases of reset on MCU controller chip. These cases of reset occurrence are below.

1. Power On Reset(POR)/Power Down Reset(PDR) (normal mode)
   - ◆ POR (VDD ≥ 2.4V) and PDR (VDD ≤ 2.35V)
2. Low Voltage Reset (LVR supports 4 levels)
   - ◆ LVR0 (VDD ≤ 2.7V Default)
   - ◆ LVR1 (VDD ≤ 3.0V)
   - ◆ LVR2 (VDD ≤ 3.6V)
   - ◆ LVR3 (VDD ≤ 4.3V)
3. Watchdog Reset
   - ◆ WDR (Watchdog Timer occur time out)
4. External Reset(PA[2])
   - ◆ EXTR (PA[2] low active)
5. Power Down Reset at Sleep mode (PDRS)
   - ◆ PDRS (VDD ≤ 1.3V)

If the POR,PDR,PDRS,WDR, LVR or EXTR occurs，the chip will enter reset status. The following events take place on reset status.

- ◆ All registers are reset to their default values expect status registers.
- ◆ The status register (03h) is reset to their default value only for POR/PDR/LVR/PDRS. After reset status, program counter begins at address 0x0000

VDD ≥ 2.4V, PORN set to high (refer 4.0-1).

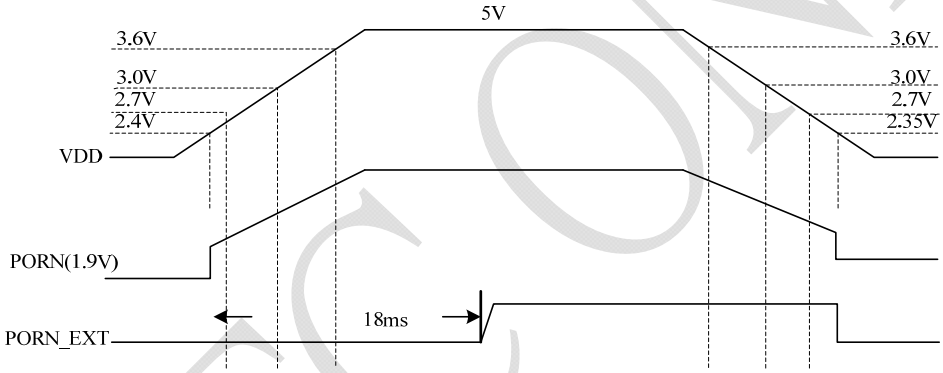


***Figure* 4.0-1 POR and LVR Sequence**

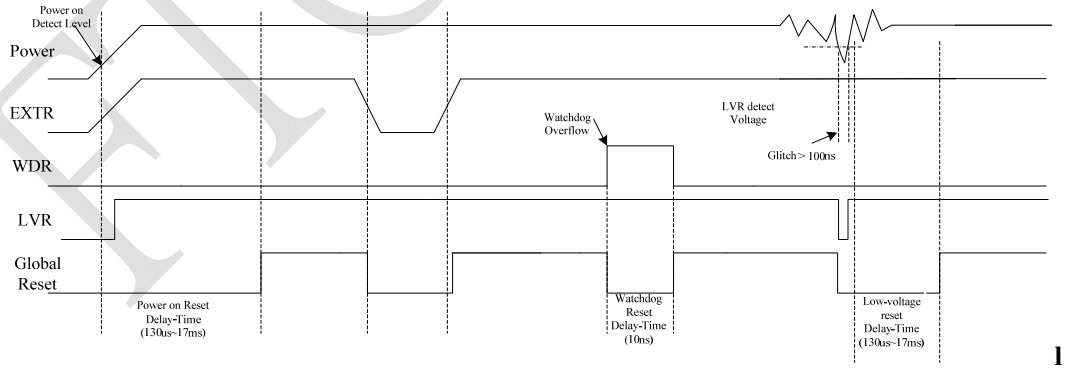


***Figure* 4.0-2 Global Sequence**

4.5 PWM Description

FM8PC75AM built in 6 PWM generators, supports 2 modes: (1)8-but, (2) 16-bit.

4.5-1 8-bit mode

8-bit mode (PWM0, PWM1, PWM2, PWM3, PWM4, and PWM5): PWM output timing as shown below Figure4.5-1.1.

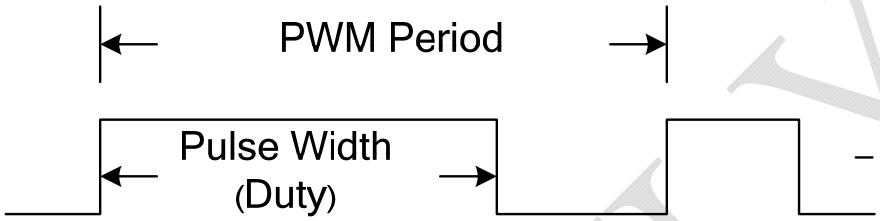


***Figure* 4.5-1.1 8-bit mode PWM output timing**

PWM0 pulse width (Duty) = ((PWM0_Duty[7:0]) == PWM0 8-bit counter);
PWM0 period = ((PWM0_PR[7:0]) == PWM0 8-bit counter);
PWM1 pulse width (Duty) = ((PWM1_Duty[7:0]) == PWM1 8-bit counter);
PWM1 period = ((PWM1_PR[7:0]) == PWM1 8-bit counter);
PWM2 pulse width (Duty) = ((PWM2_Duty[7:0]) == PWM2 8-bit counter);
PWM2 period = ((PWM2_PR[7:0]) == PWM2 8-bit counter);
PWM3 pulse width (Duty) = ((PWM3_Duty[7:0]) == PWM3 8-bit counter);
PWM3 period = ((PWM3_PR[7:0]) == PWM3 8-bit counter);
PWM4 pulse width (Duty) = ((PWM4_Duty[7:0]) == PWM4 8-bit counter);
PWM4 period = ((PWM4_PR[7:0]) == PWM4 8-bit counter);
PWM5 pulse width (Duty) = ((PWM5_Duty[7:0]) == PWM5 8-bit counter);
PWM5 period = ((PWM5_PR[7:0]) == PWM5 8-bit counter);

8-bit PWM clock as shown below Figure4.5-1.2.

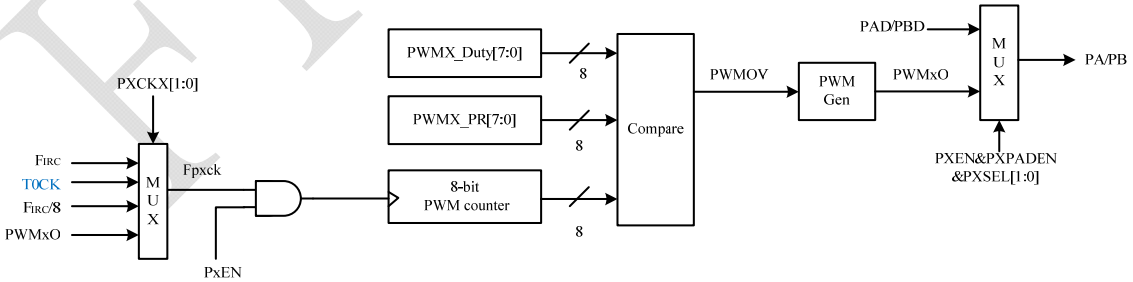


***Figure* 4.5-1.2 8-bit PWM Block Diagram**

4.5-2 16-bit mode (single phase output)

PWM output timing as shown below Figure 4.5-2

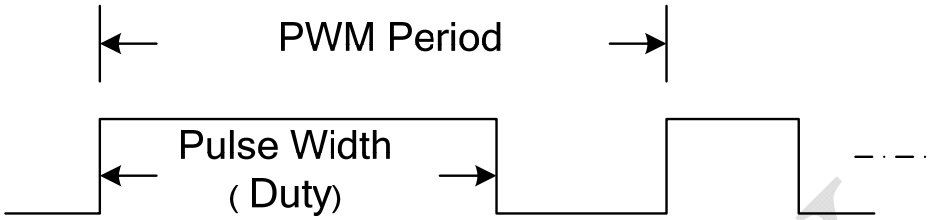


***Figure* 4.5-2.1 16-bit PWM output timing**

PWM01 pulse width (Duty) = ({PWM1_Duty[7:0], PWM0_Duty[7:0]}) == PWM01 16-bit counter);
PWM23 pulse width (Duty) = ({PWM3_Duty[7:0], PWM2_Duty[7:0]}) == PWM23 16-bit counter);
PWM45 pulse width (Duty) = ({PWM5_Duty[7:0], PWM4_Duty[7:0]}) == PWM45 16-bit counter);
PWM01 period = ({PWM1_PR[7:0], PWM0_PR[7:0]) == PWM01 16-bit counter);
PWM23 period = ({PWM3_PR[7:0], PWM2_PR[7:0]) == PWM23 16-bit counter);
PWM45 period = ({PWM5_PR[7:0], PWM4_PR[7:0]) == PWM45 16-bit counter);
PWM01,PWM23,PWM45 16-位计数器時鐘： HIRC,T0CK,HIRC/8

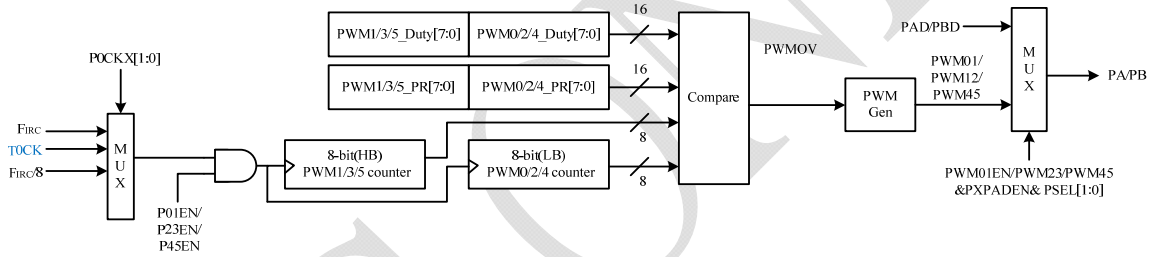
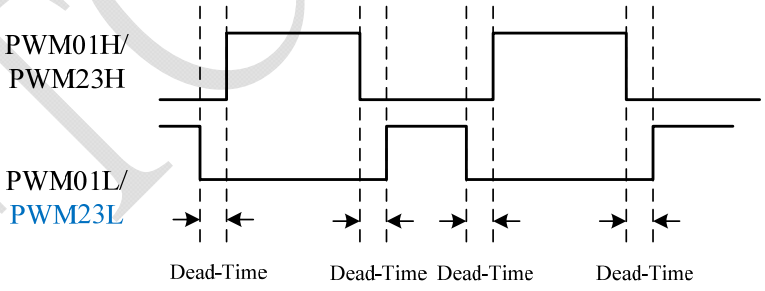


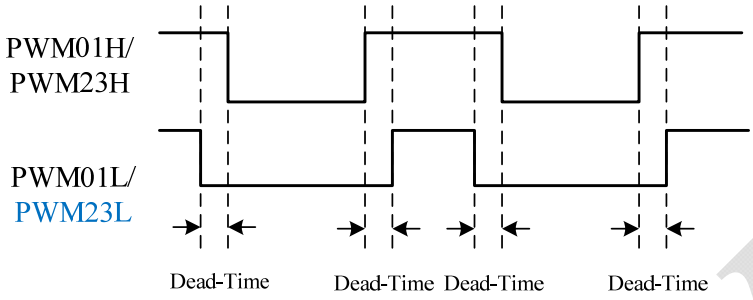
***Figure* 4.5-2.2 16-bit PWM Block Diagram**

4.5-2 16-bit mode (tow phase same/reverse output)

4.5-2_1 PWM01/23 reverse output



4.5-2_1 PWM01/23 same output



4.5-3 PWM sample

PWM01, 16bit

```
Step1:  Set Period and Duty
        MOVIA   00H             ; PWM01 100/200
        MOVAR   PWM0_Duty
        MOVAR   PWM0_PR
        MOVAR   PWM01CON        ; PWM clock = FIRC (16M/8M by writer's option)
        MOVIA   01H
        MOVAR   PWM1_Duty
        MOVIA   02H             ; assume FIRC = 16Mhz
        MOVAR   PWM1_PR         ; Period = 32us (62.5ns * 512), Duty = 16us (62.5ns * 128)
Step2:  Set output pin
        CLRR    PWMOSL          ; PWM01 output = PA3
        MOVIA   01H
        MOVAR   PWMPADEN        ; enable output function
Step3:  Enable PWM & PWM Interrupt      ; interrupt is non-essential
        CLRA
        IOST    PSEL            ; select PWM interrupt when Duty occurs
        BSR     PWMINTEN,0      ; enable PWM01 interrupt
        BSR     INTEN,7         ; enable GIE
        MOVIA   41H
        MOVIA   PWMEN           ; enable PWM01
```

PWM0, 8bit

```
Step1:  Set Period and Duty
        MOVIA   40H             ; PWM0 40/BF
        MOVAR   PWM0_Duty
        MOVIA   BFH
        MOVAR   PWM0_PR
Step2:  Set output pin
        CLRR    PWMOSL          ; PWM0 output = PA3
        MOVIA   01H
        MOVAR   PWMPADEN        ; enable output function
Step3:  Enable PWM
        MOVIA   01H
        MOVIA   PWMEN           ; enable PWM0
```

4.6 Channel Analog to Digital(ADC)

Build in ADC module supports 6+2 channel (PB[0]~PB[5]) and one internal channel ¼ VDD reference that can be use for auxiliary input ,battery monitor and temperature monitor. The ADC module converts an input voltage to a 12-bit digital code.

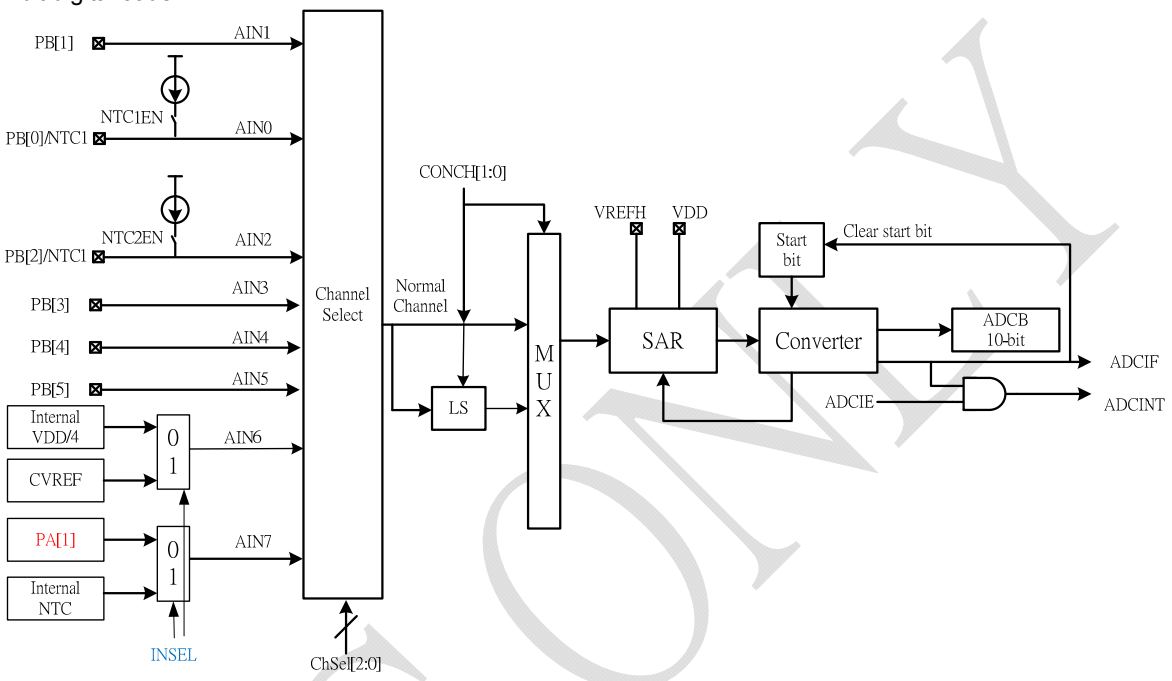


***Figure* 4.6-1 ADC block diagram**

4.6-1 ADC Current Direction Example

Method 1:

Step1 : Set CHSEL[3:0] = 3'b000(AIN = PB0)

Step2 : Set CONCH[1:0] = 2'b11

Step3 : Read ADC[11:0] = 12'h666 (for example : ADC =666h)

- AIN = VSS + V_{LS}(0.8V)

Step4 : set CONCH[1:0] = 2'b10

Step5 : Read ADC[11:0] = 12'hNEW

- AIN = PB0 + V_{LS}(0.8V)
  - 12h'NEW > 12'h666(PB0 > VSS)
  - 12h'NEW < 12'h666(PB0 < VSS)

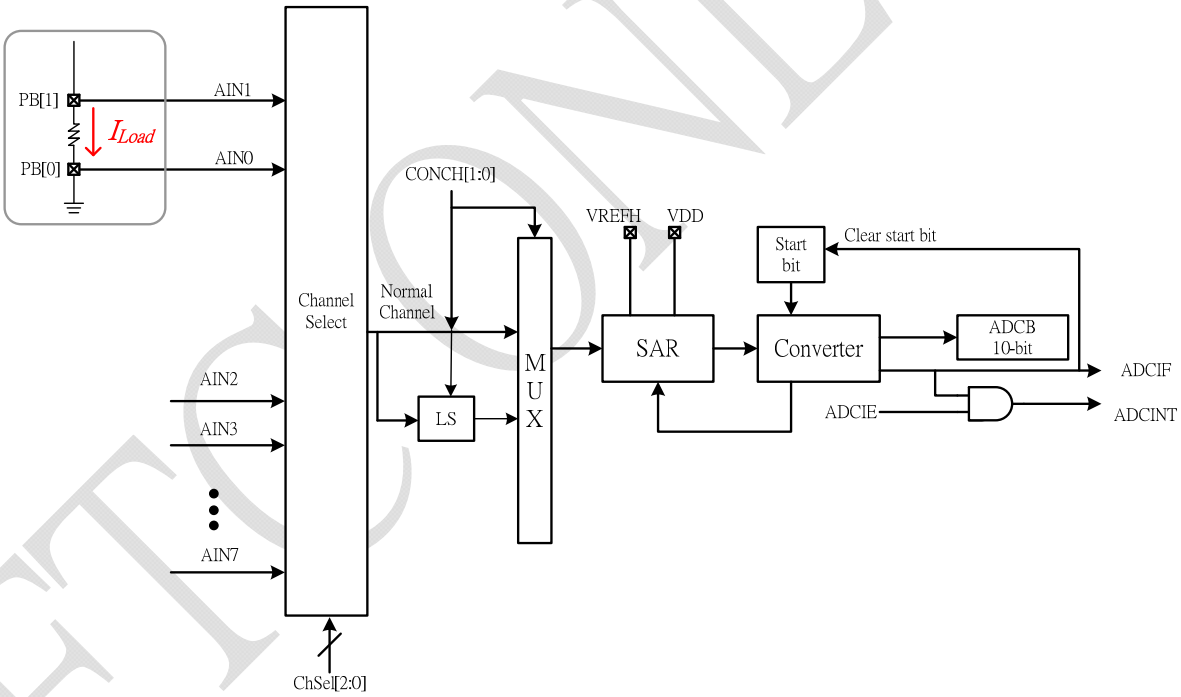


***Figure* 4.6-2 ADC current direction detect diagram**

Method 2:

Step1 : Set SELVER[2:0] = 3b'011(VREFH = 2V)

Step2 : Set CHSEL[2:0] = 3'b000

Step3 : set CONCH[1:0] = 2'b10

Step4 : Read ADC[11:0] = $ADC_{(0)}$

- AIN = PB0 + V_{LS}(0.8V)

Step5 : set CHSEL[2:0] = 3'b001

Step6 : Read ADC[11:0] = $ADC_{(1)}$

- $ADC_{(1)}$ > $ADC_{(0)}$
  - PN1 > PB0(VSS)，positive current direction
- $ADC_{(1)}$ < $ADC_{(0)}$
  - PN1 < PB0(VSS)，negative current direction
  - NOTE: V- cannot less VSS exceed 0.3V

4.7 Temperature Sensor Detect (TSD)

FM8PC75AM supports two external temperature Sensor Detectors (NTC1, NTC2) and an internal negative temperature coefficient sensor.

Temperature detect can use ADC channel or comparator channel occurs interrupt. ,as shown Figure 4.7-1.

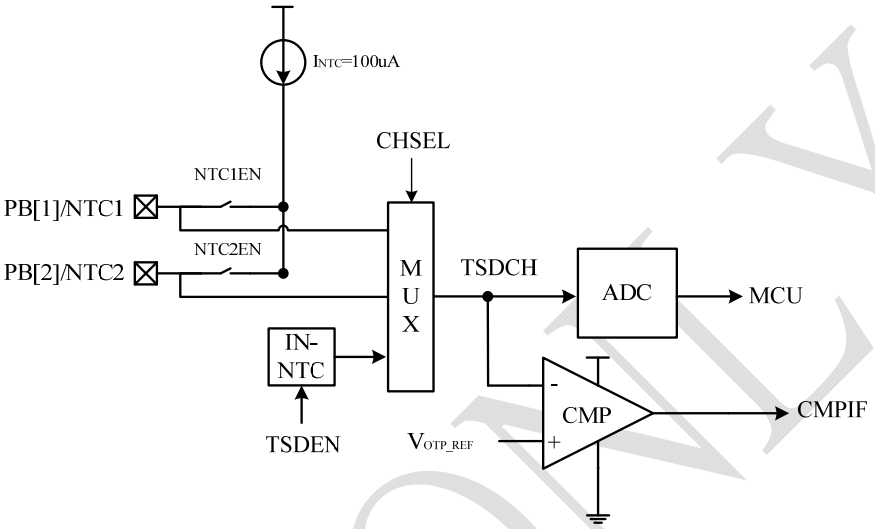


***Figure* 4.7-1 Temperature detect block diagram**

4.7-1 NTC/TSD Example

```
Step1:  Set VOTPSL[1:0]                  ; Select internal compare Voltage 1V or 0.5V
Step2:  Set {NTC1EN, NTC2EN, TSDEN}      ; Select external NTC or internal NTC
Step3:  Set CM[2:0] = 101                ; Set COPCON1, enable comparator
```

4.8 Voltage Comparator

FM8PC75AM build in one voltage comparator, the block diagram as follow Figure 4.8-1.
(1) Compare by two external pin.
(2) Compare by internal reference voltage (VREF=1V from Bandgap) and external pin.
(3) Compare by internal vdd reference voltage (CVREF) and external pin.
(4) Compare by internal vdd reference voltage (CVREF) and internal reference voltage (VREF=1V).

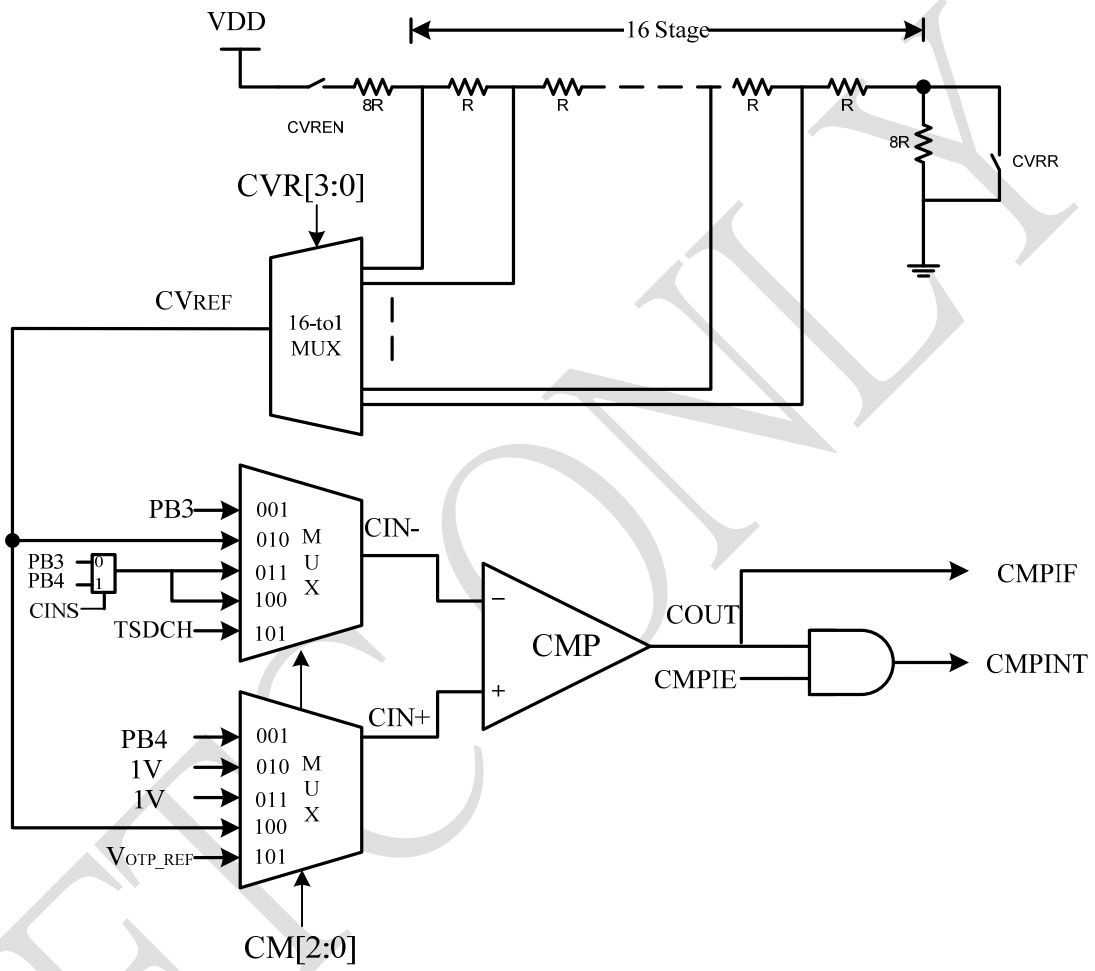


***Figure* 4.8-1 Comparator block diagram**

If CVRR = 1 and CVREN=1: CVREF = CVR[3:0] * Vdd / 18.

If CVRR = 0 and CVREN=1: CVREF = Vdd / 10 + CVR[3:0] * Vdd / 20.

4.9 I/O PAD

Ports A is 8-bit data input/output register，Ports B is 6-bit data input/output register，each pan can support wake-up function as shown Figure 4.9-1. Each I/O pin has a corresponding register bit (IOSTA, IOSTB) to define it is input or output pin.
When an I/O pin is configured as input pin (high-impedance), it may has pull-high resistor.
When an I/O pin is configured as output pin, there is a corresponding register bit to select as drive pad or sink pad.
After reset, IOSTA and IOSTB are cleared, GPIO as input mode。

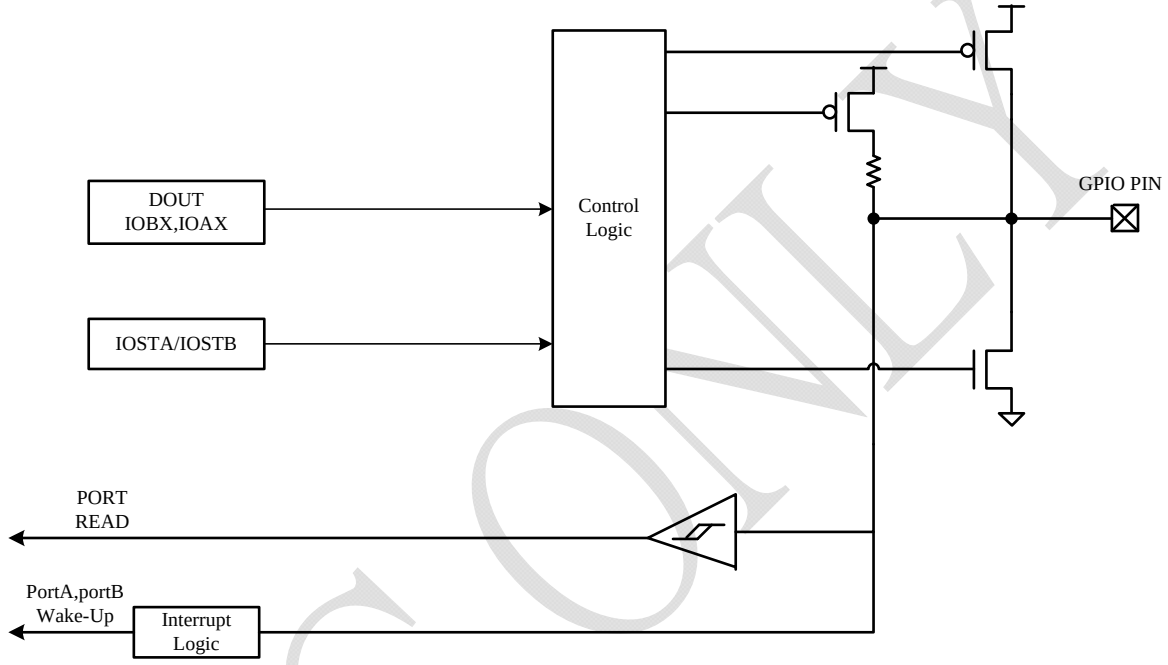


***Figure* 4.9-1 I/O pad block diagram**

4.10 Operating mode

	Normal	Sleep	Green Mode
HIRC	By Program	Off	Off
SIRC	By Program	Off	On
LVDT	By Program	Off	Off
CPU	Operating	Off	Off
Wake up	-	By Program	By Program
WDT reset	By Program	No	By Program

4.11 interrupt Function

FM8PC75AM supports fellow interrupts:
(1) PWM interrupts
(2) Timer1,Timer2 and Timer3 interrupts
(3) INT0 external interrupt
(4) ADC completed interrupt
(5) Comparator output changed interrupt
(6) Low voltage detect interrupt (LVDT)

The reset vector for FM8PC75AM is at **0x0000h**, and interrupt vector is at **0x0008h.**
Global interrupt enable bit = 0 (**GIE** at Reg.0Eh-7) can disable all interrupts. When an interrupt event occur with the GIE bit and its corresponding interrupt enable bit are all set, the GIE bit will be cleared by hardware to disable any further interrupts. The RETFIE instruction will exit the interrupt routine and set the GIE bit to re-enable interrupt.

【5】 Data Register Descriptions

5.1 Indirect Addressing

The INDF Register is not a physical register. Any instruction accessing the INDF register can actually access the register pointed by FSR Register. Reading the INDF register itself indirectly (FSR="0") will read 00h. Writing to the INDF register indirectly results in a no-operation (although status bits may be affected).
The bits of FSR register [6:0] are used to select up to 128 registers (address 00h ~ 7Fh).

Address 00H : Indirect addressing (INDF)

Read/Write-POR		R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x00	INDF	B7	B6	B5	B4	B3	B2	B1	B0

INDF uses contents of FSR to address data memory (not a physical register).

Address 04H : Indirect Data Memory Address Pointer Register (FSR)

Read/Write-POR		R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x04	FSR	GP	F6	F5	F4	F3	F2	F1	F0

Example:
(1) Write 0xAA to Address 7Fh Register

```
MOVIA    7Fh
MOVAR    FSR        ; Pointer = 7Fh
MOVIA    AAh
MOVAR    INDF       ; Write AAh to Address = 7Fh Register
```

(2) Read Address 7Fh Register to ACC

```
MOVIA    7Fh
MOVAR    FSR        ; Pointer = 7Fh
MOVR     INDF,A     ; Read Address from 7Fh Register to ACC
```

5.2 Program Counter

Address 01H: Program Counter High byte (PCH)

Read/Write-POR		R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x01	PCH	-	-	-	-	-	HB2	HB1	HB0

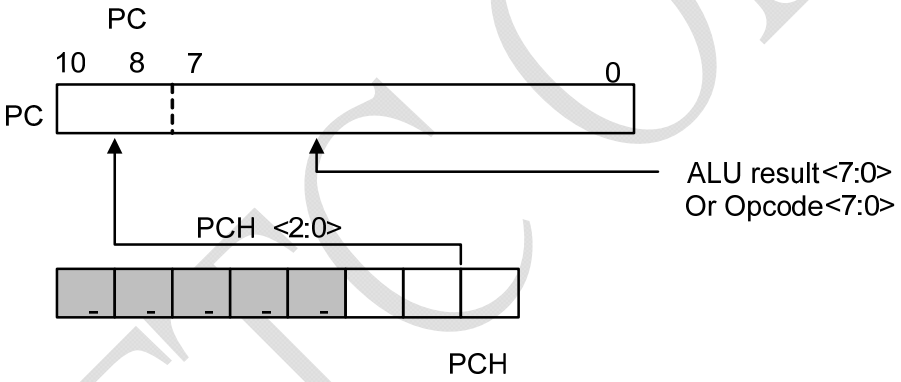
For any instruction where the PCL is the destination, the PC<7:0> is provided by the instruction word. However, the PC<10:8> will come from the PCHBUF<2:0> register (PCH <2:0> → PC<10:8>).

Address 02H: Program Counter Low byte (PCL)

Read/Write-POR		R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x02	PCL	LB7	LB6	LB5	LB4	LB3	LB2	LB1	LB0

FM8PC75AM device has a 11-bit wide Program Counter (PC) and five-level deep 11-bit hardware push/pop stack. The low byte of PC is called the PCL register. This register is readable and writable. The high byte of PC is called the PCH register. This register contains the PC<9:8> bits and is not directly readable or writable. All updates to the PC<10:8> go through the PCH register. As a program instruction is executed, the Program Counter will contain the address of the next program instruction to be executed. The PC value is increased by one, every instruction cycle, unless an instruction changes the PC.
For any instruction where the PCL is the destination, the PC<7:0> is provided by the instruction word or ALU result. However, the PC<10:8> will come from the PCH<2:0> bits (PCH <2:0> → PC<10:8>).

Example: Instruction with PCL as destination



5.3 Status Register

This register contains the arithmetic status of the ALU, the RESET status.
If the STATUS Register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled.

Address 03H: Status Register (STATUS)

Read/Write-POR		R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x03	STATUS	RST	RESTORE	RAMBK	$\overline{TO}$	$\overline{PD}$	Z	DC	C

Bit[7]: RST
Wake up type Bit
1 = Wake up
0 = System reset (power on, brown out, MCLRB, WDT time out).

Bit[6] : RESTORE Bit
1 = RETFIE cannot restore ACC[7:0], FSR[6:0], PCH[2:0] and STATUS[5][2:0].
0 = RETFIE auto restore ACC[7:0], FSR[6:0], PCH[2:0] and STATUS[5][2:0].

Bit[5] : RAMBK Bit
1 : Select RAM Bank-1
0 : Select RAM Bank-0

Bit[4] : /TO
WDT Overflow Bit
1 = Power on reset, brown reset, CLRWDT and SLEEP instruction
0 = WDT Overflow reset

Bit[3] : /PD
Power down bit
1 = Power on reset, brown reset and CLRWDT instruction
0 = SLEEP instruction

Bit[2] : Z
Zero bit.
1 = The result of a logic operation is zero.
0 = The result of a logic operation is not zero.

Bit[1] : DC
Half carry/half borrow bit.
ADDAR, ADDIA, ADCAR, ADCIA
1 = A carry from the 4th low order bit of the result occurred.
0 = A carry from the 4th low order bit of the result did not occur.
SUBAR, SUBIA, SBCAR, SBCIA
1 = A borrow from the 4th low order bit of the result did not occur.
0 = A borrow from the 4th low order bit of the result occurred

Bit[0] : C
Carry/borrow bit.
ADDAR, ADDIA, ADCAR, ADCIA,
1 = A carry occurred.
0 = A carry did not occur.
SUBAR, SUBIA, SBCAR, SBCIA
1 = A borrow did not occur.
0 = A borrow occurred.

5.4 I/O PAD Register

Ports A is an 8-bit port data register. Ports B is a 6-bit port data register. Reading the port (PORTA, PORTB register) reads the status of the pins independent of the pin's input/output modes. Writing to these ports will write to the port data latch.

Address 05H: PORTA I/O Status Register (IOSTA)

Read/Write-POR		R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x05	IOSTA	IOSTA7	IOSTA6	IOSTA5	IOSTA4	IOSTA3	IOSTA2	IOSTA1	IOSTA0

Bit[7] : IOSTA7
PORTA[7] I/O bit
1 = IN
0 = Output

Bit[6] : IOSTA6
PORTA[6] I/O bit
1 = IN
0 = Output

Bit[5] : IOSTA5
PORTA[5] I/O bit
1 = IN
0 = Output

Bit[4] : IOSTA4
PORTA[4] I/O bit
1 = IN
0 = Output

Bit[3] : IOSTA3
PORTA[3] I/O bit
1 = IN
0 = Output

Bit[2] : IOSTA2
PORTA[2] I/O bit
1 = IN
0 = Output

Bit[1] : IOSTA1
PORTA[1] I/O bit
1 = IN
0 = Output

Bit[0] : IOSTA0
PORTA[0] I/O bit
1 = IN
0 = Output

Address 06H: PORTA Data Register (PORTA)

Read/Write-POR		R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x06	PORTA	IOA7	IOA 6	IOA 5	IOA 4	IOA 3	IOA 2	IOA 1	IOA 0

Bit[7] : IOA**7**
PORTA[7] Data bit
1 = Output High
0 = Output Low

Bit[6] : IOA**6**
PORTA[6] Data bit
1 = Output High
0 = Output Low

Bit[5] : IOA**5**
PORTA[5] Data bit
1 = Output High
0 = Output Low

Bit[4] : IOA**4**
PORTA[4] Data bit
1 = Output High
0 = Output Low

Bit[3] : IOA**3**
PORTA[3] Data bit
1 = Output High
0 = Output Low

Bit[2] : IOA**2**
PORTA[2] Data bit
1 = No output (Open Drain)
0 = Output Low

Bit[1] : IOA**1**
PORTA[1] Data bit
1 = Output High
0 = Output Low

Bit[0] : IOA**0**
PORTA[0] Data bit
1 = Output High
0 = Output Low

Address 07H: PORTB I/O Status Register (IOSTB)

Read/Write-POR		R-0	R-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x07	IOSTB	-	-	IOSTB5	IOSTB4	IOSTB3	IOSTB2	IOSTB1	IOSTB0

Bit[5] : IOSTB5
PORTB[5] I/O bit
1 = IN
0 = Output

Bit[4] : IOSTB4
PORTB[4] I/O bit
1 = IN
0 = Output

Bit[3] : IOSTB3
PORTB[3] I/O bit
1 = IN
0 = Output

Bit[2] : IOSTB2
PORTB[2] I/O bit
1 = IN
0 = Output

Bit[1] : IOSTB1
PORTB[1] I/O bit
1 = IN
0 = Output

Bit[0] : IOSTB0
PORTB[0] I/O bit
1 = IN
0 = Output

Address 08H: PORTB Data Register (PORTB)

Read/Write-POR		R-0	R-0	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x08	PORTB	-	-	IOB5	IOB4	IOB3	IOB2	IOB1	IOB0

Bit[5] : IOB**5**
PORTB[5] Data Output Register
1 = Output High
0 = Output Low

Bit[4] : IOB**4**
PORTB[4] Data Output Register
1 = Output High
0 = Output Low

Bit[3] : IOB**3**
PORTB[3] Data Output Register
1 = Output High
0 = Output Low

Bit[2] : IOB**2**
PORTB[2] Data Output Register
1 = Output High
0 = Output Low

Bit[1] : IOB**1**
PORTB[1] Data Output Register
1 = Output High
0 = Output Low

Bit[0] : IOB**0**
PORTB[0] Data Output Register
1 = Output High
0 = Output Low

Address 26H: PORTA Wake up Control Register (AWUCON)

Read/Write-POR		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x26	AWUCON	AWE[7]	AWE[6]	AWE[5]	AWE[4]	AWE[3]	AWE[2]	AWE[1]	AWE[0]

Bit[7]: AWE[7]
PortA [7] wakeup enable bit
1 = Enable.
0 = Disable.

Bit[6]: AWE[6]
PortA [6] wakeup enable bit
1 = Enable.
0 = Disable.

Bit[5]: AWE[5]
PortA [5] wakeup enable bit
1 = Enable.
0 = Disable.

Bit[4]: AWE[4]
PortA [4] wakeup enable bit
1 = Enable.
0 = Disable.

Bit[3]: AWE[3]
PortA [3] wakeup enable bit
1 = Enable.
0 = Disable.

Bit[2]: AWE[2]
PortA [2] wakeup enable bit
1 = Enable.
0 = Disable.

Bit[1]: AWE[1]
PortA [1] wakeup enable bit
1 = Enable.
0 = Disable.

Bit[0]: AWE[0]
PortA [0] wakeup enable bit
1 = Enable.
0 = Disable.

Address 27H: PORTA Pull-High Control Register (APHCON)

Read/Write-POR		R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-**1**	R/W-1	R/W-1
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x27	APHCON	APH[7]	APH[6]	APH[5]	APH[4]	APH[3]	APH[2]	APH[1]	APH[0]

Bit[7]: APH[7]
PortA [7] pull high enable bit
0 = Enable.
1 = Disable.

Bit[6]: APH[6]
PortA [6] pull high enable bit
0 = Enable.
1 = Disable.

Bit[5]: APH[5]
PortA [5] pull high enable bit
0 = Enable.
1 = Disable.

Bit[4]: APH[4]
PortA [4] pull high enable bit
0 = Enable.
1 = Disable.
.

Bit[3]: APH[3]
PortA [3] pull high enable bit
0 = Enable.
1 = Disable.

Bit[2]: APH[2]
PortA [2] pull high enable bit
0 = Enable.
1 = Disable.

Bit[1]: APH[1]
PortA [1] pull high enable bit
0 = Enable.
1 = Disable.

Bit[0]: APH[0]
PortA [0] pull high enable bit
0 = Enable.
1 = Disable.

Address 28H: PORTB Wake up Control Register (BWUCON)

Read/Write-POR		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x28	BWUCON	UGMD	GreenL	BWE[5]	BWE[4]	BWE[3]	BWE[2]	BWE[1]	BWE[0]

Bit[7]: UGMD
Ultra GREEN Mode signal.
1 = SIRC (32KHz/10) Power saving mode.
0 = SIRC (32KHz).

Bit[6]: GreenL
1: enable Green Mode: LVDT Disable, Fcpu Disable.
0: disable Green Mode: MCU operating.

Bit[5]: BWE[5]
PortB [5] wakeup enable bit
1 = Enable.
0 = Disable.

Bit[4]: BWE[4]
PortB [4] wakeup enable bit
1 = Enable.
0 = Disable.

Bit[3]: BWE[3]
PortB [3] wakeup enable bit
1 = Enable.
0 = Disable.

Bit[2]: BWE[2]
PortB [2] wakeup enable bit
1 = Enable.
0 = Disable.

Bit[1]: BWE[1]
PortB [1] wakeup enable bit
1 = Enable.
0 = Disable.

Bit[0]: BWE[0]
PortB [0] wakeup enable bit
1 = Enable.
0 = Disable.

Address 29H: PORTB Pull-High ControlRegister (BPHCON)

Read/Write-POR		R/W-0	R -0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x29	BPHCON	INENPA1	-	BPH[5]	BPH[4]	BPH[3]	BPH[2]	BPH[1]	BPH[0]

Bit[7] : INENPA1
PA[1] digital input Enable.
1 = Disable (read PA[1] as 0)
0 = Enable

Bit[5]: BPH[5]
PortB [5] pull high enable bit
0 = Enable.
1 = Disable.

Bit[4]: BPH[4]
PortB [4] pull high enable bit
0 = Enable.
1 = Disable.
.

Bit[3]: BPH[3]
PortB [3] pull high enable bit
0 = Enable.
1 = Disable.
.

Bit[2]: BPH[2]
PortB [2] pull high enable bit
0 = Enable.
1 = Disable.

Bit[1]: BPH[1]
PortB [1] pull high enable bit
0 = Enable.
1 = Disable.

Bit[0]: BPH[0]
PortB [0] pull high enable bit
0 = Enable.
1 = Disable.
.

5.5 Timer Register(16 bits)

Address 09H: Timer1 Control Register (T1con)

Read/Write-POR		R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x09	T1CON	-	-	-	T1PS1	T1PS0	T1CS1	T1CS0	T1EN

Bit[4:3]: T1PS[1:0]

Timer1 clock division:

T1PS1:T1PS0	clock division
0 0	1:1
0 1	1:2
1 0	1:4
1 1	1:8

Bit[2:1]: T1CS[1:0]

Timer1 clock source

T1CS[1:0]	Clock source
2'b00	FCPU
2'b01	FIRC (16Mhz/8Mhz)
2'b10	Timer2 output
2'b11	T0CK

Bit[0] : T1EN

Timer1 Enable bit

1 = Timer1 enable.

0 = Timer1 disable

Address 0AH: Timer1 Low-byte Reload Register (TMR1LB)

Read/Write-POR		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x0A	TMR1LB	TMR1LB[7:0]							

Bit[7:0] : TM1LB[7:0]

Write data to update TMR1LB, but read data from TM1[7:0].

Address 0BH: Timer1 High-byte Reload Register (TMR1HB)

Read/Write-POR		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x0B	TMR1HB	TMR1HB[7:0]							

Bit[7:0] : TM1HB[7:0]

Write data to update TMR1HB, but read data from TM1[15:0].

Address 0CH: Internal Oscillator and Watchdog Control Register (IRCWCON)

Read/Write-POR		R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x0C	IRCWCON	WDTEN	HIRCEN	WS1	WS0	CPUS	IRCF2	IRCF1	IRCF0

Bit[7] : WDTEN

WDT enable bit
1 : Enable WDT
0 : Disable WDT

Bit[6] : HIRCEN

Internal Oscillator (HIRC) enable bit
1 : Enable internal oscillator
0 : Disable internal oscillator

Bit[5:4] : WS[1:0]

Watchdog select bits

WS[1:0]	Overflow time
2'b00	2 s
2'b01	288 ms
2'b10	72 ms
2'b11	18 ms (default)

Bit[3] : CPUS

CPU clock select bit
1 : HIRC (16M/8Mhz)
0 : SIRC (about 32Khz)

Bit[2:0] : IRCF[2: 0]

HIRC Division

IRCF[2: 0]	Fcpu division
3'b000	IRC
3'b001	IRC/2
3'b010	IRC/4
3'b011	IRC/8
3'b100	IRC/16
3'b101	IRC/32
3'b110	T0CK
3'b111	Inhibit

5.5 Low Voltage Detect Register

Address 0DH: Low Voltage Detect Control Register (LVDTCON)

Read/Write-POR		R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	R/W-**0**	R/W-1	R/W-1
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x0D	LVDTCON	EIS	RDPORT	RA2EN	LVENB	INTEDG	SEN	S1	S0

Bit[7] : EIS

External Interrupt select bit
1: IOB5= interrupt (INT0) input.
0: IOB5= general input/output pad.

Bit[6] : RDPORT

Read form port bit
1: Read Data Register 06H(PORTA) and 08H(PORTB).
0: Read PAD

Bit[5] : RA2EN

IOA2 general I/O enable bit
1: IOA2 is general I/O.
0: IOA2 is external reset pin

Bit[4] :LVENB

Low voltage reset enable bit
1: Enable low voltage reset.
0: Disable low voltage reset.

Bit[3] : INTEDG

Interrupt edge select bit
1: interrupt on rising edge of INT0 pin.
0: interrupt on falling edge of INT0 pin.

Bit[2] : SEN

PB3、PB4 Short select bit
1: PB3、PB4 short.
0: PB3、PB4 open.

Bit[1:0] :S[1:0]

Detect voltage select bits

S[1: 0]	Voltage
2'b11	2.7V(Initial Value)
2'b10	3.0V
2'b01	3.6V
2'b00	4.3V

5.5 interrupt Register

Address 0EH: interrupt Control Register (INTEN)

Read/Write-POR		R/W-0	R -0	R -0	R/W-0	R/W-0	R/W-0	R -0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x0E	INTEN	GIE	-	-	LVDTIE	CMPIE	INTIE	-	T1IE

Bit[7] :GIE
Globle interrupt enable bit
1 : Enable all interrupts
0 : Disable All interrupts

Bit[6:5] :reserved

Bit[4] : LVDTIE
Low voltage detect interrupt enable bit
1 : Enable low voltage detect interrupt
0 : Disable low voltage detect interrupt

Bit[3] : CMPIE
Comparator interrupt enable bit
1 : Enable comparator interrupt
0 : Disable comparator interrupt

Bit[2] : INTIE
External interrupt enable bit
1 : Enable external interrupt
0 : Disable external interrupt

Bit[1] : reserved

Bit[0] : T1TIE
Timer1 overflow interrupt enable bit
1 : Enable Timer1 overflow interrupt
0 : Disable Timer1 overflow interrupt

Address 0FH: interrupt flagRegister (INTFLAG)

Read/Write-POR		R -0	R -0	R -0	R/W-0	R/W-0	R/W-0	R -0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x0F	INTFLAG	-	-	-	LVDTIF	CMPIF	INTIF	-	T1IF

Bit[7:5] : reserved

Bit[4] : LVDTIF
Low voltage detect interrupt flag
1 = Interrupt occurs.
0 = LVDTIF must clear by firmware

Bit[3] : CMPIF
Comparator interrupt flag
1 = Interrupt occurs.
0 = CMPIF must clear by firmware

Bit[2] : INTIF
External interrupt flag
1 = Interrupt occurs.
0 = INTIF must clear by firmware

Bit[1] : reserved

Bit[0] : T1IF
Timer1 interrupt flag
1 = Interrupt occurs.
0 =T1IF must clear by firmware

5.6 ADC Control Register

Address 2BH: ADC Control Register1 (ADCON1)

Read/Write-POR		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x2B	ADCON1	ADCEN	ADCST	CHSEL2	CHSEL1	CHSEL0	INSEL	ADCSR1	ADCSR0

Bit[7] : ADCEN

ADC enable bit
1 = ADC enable
0 = ADC disable

Bit[6] : ADCST

1 = Start ADC, conversion has been completed, clear 0 by H/W.
0 = Stop.

Bit[5:3] : CHSEL[2:0]

ADC input channels shown as **Table 5.6-1**

CHSEL[2:0]	Input channel(**INSEL=0)**	Input channel (**INSEL=1)**
3'b000 (AIN0)	PB[0] /external-NTC1	PB[0] /external-NTC1
3'b001 (AIN1)	PB[1]	PB[1]
3'b010 (AIN2)	PB[2] /external-NTC2	PB[2] /external-NTC2
3'b011 (AIN3)	PB[3]	PB[3]
3'b100 (AIN4)	PB[4]	PB[4]
3'b101 (AIN5)	PB[5]	PB[5]
3'b110 (AIN6)	Internal VDD/4	CVREF
3'b111 (AIN7)	PA[1]	Internal INTC*

Table 5.6-1 ADC input channels select

* : negative temperature coefficient

Bit[2] : INSEL

Internal reference select bit
1 : CVREF, INTC base on CHSEL[2:0].
0 : VDD/4, PA[1] base on CHSEL[2:0].

Bit[1:0] : ADCSR[1:0]

ADC clock select
2'b00 : ADC clock = Fcpu/512
2'b01 : ADC clock = Fcpu/256
2'b10 : ADC clock = Fcpu/128
2'b11 : ADC clock = Fcpu/64

Note : VREFH=2.0V VDD >=3V , Select ADC clock >= 4us (<= 250K)
VREFH=1.2V VDD >=2.4V , Select ADC clock >= 4us (<= 250K)
VREFH=1.0V VDD >=2.4V , Select ADC clock >= 4us (<= 250K)

Address 2CH: ADC Control Register2 (ADCON2)

Read/Write-POR		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x2C	ADCON2	ADCIE	ADCIF	SVREFH	ADCNT	GP	SLVER2	SLVER1	SLVER0

Bit[7] : ADCIE
ADC Interrupt Enable
1 = Enable
0 = Disable

Bit[6] : ADCIF
ADC Interrupt Flag Bit
1 = ADC conversion has been completed, write 0 clear flag.
0 = ADC conversion has not been completed.

Bit[5] : SVREFH
Enable internal reference voltage
1 = Inhibit
0 = Enable (refer table 5.6-2).

Bit[4] : ADCNT
ADC mode
1 = ADC continuous mode
0 = ADC trigger mode , trigger by ADCST bit

Bit[3] : General Bit

Bit[2:0] : SELVER[2:0]
ADC internal VREFH voltage

ADCEN	SELVER[2:0]	VREFH
1	3'b000	VDD
	3'b001	4V
	3'b010	3V
	3'b011	2V
	3'b100	1.2V
	3'b101	1V
	3'b110	Inhibit
	3'b111	Inhibit
0	3'bxxx	Disable

Table 5.6-2 ADC internal VREFH voltage

Address 2DH: ADC Control Register3 (ADCON3)

Read/Write-POR		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x2D	ADCON-3	CONCH1	CONCH0	INEN5	INEN4	INEN3	INEN2	INEN1	INEN0

Bit[7:6] : CONCH[1:0]
ADC channel select

CONCH[1:0]	**channel**
2'b0X	CHSEL[2:0]
2'b10	External R to VSS
2'b11	Internal R to VSS

Bit[5] : INEN[5]
PB[5] digital input enable bit
1 = Disable
0 = Enable

Bit[4] : INEN[4]
PB[4] digitak input enable bit
1 = Disable
0 = Enable

Bit[3] : INEN[3]
PB[3] digital input enable bit
1 = Disable
0 = Enable

Bit[2] : INEN[2]
PB[2] digital input enable bit
1 = Disable
0 = Enable

Bit[1] : INEN[1]
PB[1] digital input enable bit
1 = Disable
0 = Enable

Bit[0] : INEN[0]
PB[0] analog digital input enable bit
1 = Disable
0 = Enable

Address 2EH: ADC Result Register High Byte (ADCHB)

Read/Write-POR		R -0	R -0	R -0	R-0	R -0	R-0	R-0	R-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x2E	ADCHB	ADCB11	ADCB10	ADCB9	ADCB8	ADCB7	ADCB6	ADCB5	ADCB4

Bit[7:0] : ADCB[11:4] read only
ADCB[11:0] higher 8bits

Address 2FH: ADC Result Register Low Nibble Byte (ADCLB)

Read/Write-POR		R/-0	R/-0	R/-0	R/-0	R-0	R -0	R0	R -0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x2F	ADCLB	-	-	-	-	ADCB3	ADCB2	ADCB1	ADCB0

Bit[3:0] : ADCB[3:0] read only
ADCB[11:0] lower 4bits

5.7 PWM Register

Address 10H: PWM Enable Register (PWMEN)

Read/Write-POR		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x10	PWMEN	P23EN	P01EN	P5EN	P4EN	P3EN	P2EN	P1EN	P0EN

Bit[7] : P23EN
PWM23 16-bit Enable.
1 = Enable
0 = Disable

Bit[6] : P01EN
PWM01 16-bit Enable
1 = Enable
0 = Disable

Bit[5] : P5EN
PWM5 8-bit Enable
1 = Enable
0 = Disable

Bit[4] : P4EN
PWM4 8-bit Enable
1 = Enable
0 = Disable

Bit[3] : P3EN
PWM3 8-bit Enable
1 = Enable
0 = Disable

Bit[2] : P2EN
PWM2 8-bit Enable
1 = Enable
0 = Disable

Bit[1] : P1EN
PWM1 8-bit Enable
1 = Enable
0 = Disable

Bit[0] : P0EN
PWM0 8-bit Enable
1 = Enable
0 = Disable

Address 11H: PWM Output Pad Enable Register-2 (PWMPADEN)

Read/Write-復位初值		R -0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x11	PWMPADEN	-	P45EN	P5PADEN	P4PADEN	P3PADEN	P2PADEN	P1PADEN	P0PADEN

Bit[6] : P45EN
PWM45 16bit Enable.
1 = Enable
0 = Disable

Bit[5] : P5PADEN
PWM5 Output Enable (**PB[5]**) .
1 = Enable
0 = Disable

Bit[4] : P4PADEN
PWM4/PWM45 Output Enable **(PA[7])**.
1 = Enable
0 = Disable

Bit[3] : P3PADEN
PWM3 Output Enable, P3SEL[1:0] select pad
1 = Enable
0 = Disable

Bit[2] : P2PADEN
PWM2/PWM23 Output Enable, P2SEL[1:0] select pad
1 = Enable
0 = Disable

Bit[1] : P1PADEN
PWM1 Output Enable, P1SEL[1:0] select pad
1 = Enable
0 = Disable

Bit[0] : P0PADEN
PWM0/PWM01 Output Enable, P0SEL[1:0] select pad
1 = Enable
0 = Disable

Address 2AH: PWM Output Pad Select Register(PWMOSL)

Read/Write-POR		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x2A	PWMOSL	P3SEL[1:0]		P2SEL[1:0]		P1SEL[1:0]		P0SEL[1:0]	

Bit[7:6] : P3SEL[1:0]

PWM3 Output select

	P3SEL[1:0]	Output Pad (PXEN)
PWM3	2'b00	PA[6] (P3EN=1, P23EN=0,P3PADEN=1)
PWM3	2'b01	PB[0] (P3EN=1, P23EN=0,P3PADEN=1)
PWM3	2'b10	PB[1] (P3EN=1, P23EN=0,P3PADEN=1)
PWM3	2'b11	PB[2] (P3EN=1, P23EN=0,P3PADEN=1)

Bit[5:4] : P2SEL[1:0]

PWM2/PWM23 Output select

	P2SEL[1:0]	Output Pad (PXEN)
PWM2 (8 Bit)	2'b00	PA[5] (P2EN=1, P23EN=0,P2PADEN=1)
PWM23(16 Bit)		PA[5] (P2EN=1 ,P3EN=X, P23EN=1 ,P2PADEN=1)
PWM2 (8 Bit)	2'b01	PB[0] (P2EN=1, P23EN=0,P2PADEN=1)
PWM23(16 Bit)		PB[0] (P2EN=X ,P3EN=X, P23EN=1, P2PADEN=1)
PWM2 (8 Bit)	2'b10	PB[1] (P2EN=1, P23EN=0,P2PADEN=1)
PWM23H(16 bit)*		PA[5] (P2EN=1 ,P3EN=X ,P23EN=1, P2PADEN=1)
PWM23L(16 Bit)*		PA[6] (P2EN=1 ,P3EN=X ,P23EN=1, P2PADEN=1)
PWM2 (8 Bit)	2'b11	PB[2] (P2EN=1, P23EN=0,P2PADEN=1)
PWM23H(16 Bit)*		PB[1] (P2EN=1 ,P3EN=X ,P23EN=1, P2PADEN=1)
PWM23L(16 Bit)*		PB[0] (P2EN=1 ,P3EN=X ,P23EN=1, P2PADEN=1)

* Complementary output PWM23H = PWM23, PWM23L = PWM23/~(PWM23) base on P2Pole[1:0], P3Pole[1:0].

Bit[3:2] : P1SEL[1:0]

PWM1 Output select

	P1SEL[1:0]	Output Pad (PXEN)
PWM1	2'b00	PA[4] (P1EN=1, P01EN=0,P1PADEN=1)
PWM1	2'b01	PA[0] (P1EN=1, P01EN=0,P1PADEN=1)
PWM1	2'b10	PA[1] (P1EN=1, P01EN=0,P1PADEN=1)
PWM1	2'b11	PB[0] (P1EN=1, P01EN=0,P1PADEN=1)

Bit[1:0] : P0SEL[1:0]

PWM0/PWM01 Output select

	P0SEL[1:0]	Output Pad (PXEN)
PWM0 (8 Bit)	2'b00	PA[3] (P0EN=1, P01EN=0,P0PADEN=1)
PWM01(16 Bit)		PA[3] (P0EN=1, P1EN=X,P01EN=1, P0PADEN=1)
PWM0 (8 Bit)	2'b01	PA[0] (P0EN=1, P01EN=0,P0PADEN=1)
PWM01(16 Bit)		PA[0] (P0EN=1, P1EN=X ,P01EN=1, P0PADEN=1)
PWM01H(16 Bit)*	2'b10	PA[3] (P0EN=1, P1EN=X ,P01EN=1, P0PADEN=1)
PWM01L(16 Bit)*		PA[4] (P0EN=1, P1EN=X ,P01EN=1, P0PADEN=1)
PWM0 (8 Bit)	2'b11	PB[0] (P0EN=1 , P01EN=0,P0PADEN=1)
PWM01H(16 Bit)*		PB[1] (P0EN=1, P1EN=X ,P01EN=1 ,P0PADEN=1)
PWM01L(16 Bit)*		PB[0] (P0EN=1, P1EN=X ,P01EN=1 ,P0PADEN=1)

* Complementary output PWM01H = PWM01, PWM01L = PWM01/~(PWM01) base on P0Pole[1:0], P1Pole[1:0].

Address 12H: PWM0/1 Control Register (PWM01CON)

Read/Write-POR		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x12	PWM01CON	P1CK1	P1CK0	P1Pole1	P1Pole0	P0CK1	P0CK0	P0Pole1	P0Pole0

Bit[7:6] : P1CK[1:0]
PWM1 clock source
= 00 : Firc(16/8MHz, by writer)
= 01 : T0CK
= 10 : Firc/8(2/1MHz)
= 01 : PWM0 output

Bit[5:4] : P1Pole[1:0]
PWM1 initial output
= 00 : Initial low output
= 01 : Initial high output
= 10 : Keep DC-low output
= 01 : Keep DC-high output

Bit[3:2] : P0CK[1:0]
PWM0 clock source
= 00 : Firc(16/8MHz)
= 01 : T0CK
= 10 : Firc/8(2/1MHz)
= 01 : PWM1 output

Bit[1:0] : P0Pole[1:0]
PWM0 initial output
= 00 : Initial low output
= 01 : Initial high output
= 10 : Keep DC-low output
= 01 : Keep DC-high output

Address 13H: PWM2/3 Control Register (PWM23CON)

Read/Write-POR		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x13	PWM23CON	P3CK1	P3CK0	P3Pole1	P3Pole0	P2CK1	P2CK0	P2Pole1	P2Pole0

Bit[7:6] : P3CK[1:0]
PWM3 clock source
= 00 : Firc(16/8MHz)
= 01 : T0CK
= 10 : Firc/8(2/1MHz)
= 01 : PWM2 output

Bit[5:4] : P3Pole[1:0]
PWM3 initial output
= 00 : Initial low output
= 01 : Initial high output
= 10 : Keep DC-low output
= 01 : Keep DC-high output

Bit[3:2] : P2CK[1:0]
PWM2 clock source
= 00 : Firc(16/8MHz)
= 01 : T0CK
= 10 : Firc/8(2/1MHz)
= 01 : PWM3 output

Bit[1:0] : P2Pole[1:0]
PWM2 initial output
= 00 : Initial low output
= 01 : Initial high output
= 10 : Keep DC-low output
= 01 : Keep DC-high output

Address 14H: PWM4/5 Control Register (PWM45CON)

Read/Write-POR		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x14	PWM45CON	P5CK1	P5CK0	P5Pole1	P5Pole0	P4CK1	P4CK0	P4Pole1	P4Pole0

Bit[7:6] : P5CK[1:0]
PWM5 clock source
= 00 : Firc(16/8MHz)
= 01 : T0CK
= 10 : Firc/8(2/1MHz)
= 01 : PWM4 output

Bit[5:4] : P5Pole[1:0]
PWM5 initial output
= 00 : Initial low output
= 01 : Initial high output
= 10 : Keep DC-low output
= 01 : Keep DC-high output

Bit[3:2] : P4CK[1:0]
PWM4 clock source
= 00 : Firc(16/8MHz)
= 01 : T0CK
= 10 : Firc/8(2/1MHz)
= 01 : PWM5 output

Bit[1:0] : P4Pole[1:0]
PWM4 initial output
= 00 : Initial low output
= 01 : Initial high output
= 10 : Keep DC-low output
= 01 : Keep DC-high output

Address 10H:PWM interrupt Select Register (PSEL)

Read/Write-POR		R/W-x	R/W-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x10	PSEL	-	-	PS5	PS4	PS3	PS2	PS1	PS0

Access by IOST/IOSTR instruction

Bit[5] : PS5
PWM5 interrupt selection
1 = interrupt when (PWM Timer == duty).
0 = interrupt when (PWM Timer == period)

Bit[4] : PS4
PWM4/PWM45 interrupt selection
1 = interrupt when (PWM Timer == duty).
0 = interrupt when (PWM Timer == period)

Bit[3] : PS3
PWM3 interrupt selection
1 = interrupt when (PWM Timer == duty).
0 = interrupt when (PWM Timer == period)

Bit[2] : PS2
PWM2/PWM23 interrupt selection
1 = interrupt when (PWM Timer == duty).
0 = interrupt when (PWM Timer == period)

Bit[1] : PS1
PWM1 interrupt selection
1 = interrupt when (PWM Timer == duty).
0 = interrupt when (PWM Timer == period)

Bit[0] : PS0
PWM0/PWM01 interrupt selection
1 = interrupt when (PWM Timer == duty).
0 = interrupt when (PWM Timer == period)

Address 24H:PWM interrupt enableRegister (PWMINTEN)

Read/Write-POR		-	-	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x24	PWMINTEN	-	-	P5IEN	P4IEN	P3IEN	P2IEN	P1IEN	P0IEN

Bit[5] : P5IEN
PWM5 interrupt enable.
1 = Enable
0 = Disable

Bit[4] : P4IEN
PWM4/PWM45 interrupt enable.
1 = Enable
0 = Disable

Bit[3] : P3IEN
PWM3 interrupt enable.
1 = Enable
0 = Disable

Bit[2] : P2IEN
PWM2/PWM23 interrupt enable.
1 = Enable
0 = Disable

Bit[1] : P1IEN
PWM1 interrupt enable.
1 = Enable
0 = Disable

Bit[0] : P0IEN
PWM0/PWM01 interrupt enable.
1 = Enable
0 = Disable

Address 25H:PWM interrupt flag Register (PWMINTFLAG)

Read/Write-POR		-	-	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x25	PWMINTFLAG	-	-	P5IF	P4IF	P3IF	P2IF	P1IF	P0IF

Bit[5] : P5IF
PWM5 interrupt flag.
1 = Interrupt occur
0 = P5IF must clear by firmware

Bit[4] : P4IF
PWM4/PWM45 interrupt flag.
1 = Interrupt occur
0 = P4IF must clear by firmware

Bit[3] : P3IF
PWM3 interrupt flag.
1 = Interrupt occur
0 = P3IF must clear by firmware

Bit[2] : P2IF
PWM2/PWM23 interrupt flag.
1 = Interrupt occur
0 = P2IF must clear by firmware

Bit[1] : P1IF
PWM1 interrupt flag.
1 = Interrupt occur
0 = P1IF must clear by firmware

Bit[0] : P0IF
PWM0/PWM01 interrupt flag.
1 = Interrupt occur
0 = P0IF must clear by firmware

Address 15H: PWM0 Duty Register (PWM0Duty)

Read/Write-POR		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x15	PWM0Duty	P0D7	P0D6	P0D5	P0D4	P0D3	P0D2	P0D1	P0D0

Bit[7:0] : P0D[7:0]

PWM0 Duty Register.
Or PWM01 low-byte Duty Register

Address 16H: PWM1 Duty Register (PWM1Duty)

Read/Write-POR		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x16	PWM1Duty	P1D7	P1D6	P1D5	P1D4	P1D3	P1D2	P1D1	P1D0

Bit[7:0] : P1D[7:0]

PWM1 Duty Register.
Or PWM01high-byte Duty Register

Address 17H: PWM2 Duty Register (PWM2Duty)

Read/Write-POR		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x17	PWM2Duty	P2D7	P2D6	P2D5	P2D4	P2D3	P2D2	P2D1	P2D0

Bit[7:0] : P2D[7:0]

PWM2 Duty Register.
Or PWM23 low-byte Duty Register

Address 18H: PWM3 Duty Register (PWM3Duty)

Read/Write-POR		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x18	PWM3Duty	P3D7	P3D6	P3D5	P3D4	P3D3	P3D2	P3D1	P3D0

Bit[7:0] : P3D[7:0]

PWM3 Duty Register.
Or PWM23 high-byte Duty Register

Address 19H: PWM4 Duty Register (PWM4Duty)

Read/Write-POR		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x19	PWM4Duty	P4D7	P4D6	P4D5	P4D4	P4D3	P4D2	P4D1	P4D0

Bit[7:0] : P4D[7:0]

PWM4 Duty Register.
Or PWM45 low-byte Duty Register

Address 1AH: PWM5 Duty Register (PWM5Duty)

Read/Write-POR		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x1A	PWM5Duty	P5D7	P5D6	P5D5	P5D4	P5D3	P5D2	P5D1	P5D0

Bit[7:0] : P5D[7:0]

PWM5 Duty Register.
Or PWM45 high-byte Duty Register

Address 1BH: PWM0 Period Register (PWM0PR)

Read/Write-POR		R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x1B	PWM0PR	P0PR[7:0]							

Bit[7:0] : P0PR[7:0]

PWM0 Period Register.

Or PWM01 low-byte Period Register

Address 1CH: PWM1 Period Register (PWM1PR)

Read/Write-POR		R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x1C	PWM1PR	P1PR[7:0]							

Bit[7:0] : P1PR[7:0]

PWM1 Period Register.

Or PWM01 high-byte Period Register

Address 1DH: PWM2 Period Register (PWM2PR)

Read/Write-POR		R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x1D	PWM2PR	P2PR[7:0]							

Bit[7:0] : P2PR[7:0]

PWM2 Period Register.

Or PWM23 low-byte Period Register

Address 1EH: PWM3 Period Register (PWM3PR)

Read/Write-POR		R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x1E	PWM3PR	P3PR[7:0]							

Bit[7:0] : P3PR[7:0]

PWM3 Period Register.

Or PWM23 high-byte Period Register

Address 1FH: PWM4 Period Register (PWM4PR)

Read/Write-POR		R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x1F	PWM4PR	P4PR[7:0]							

Bit[7:0] : P4PR[7:0]

PWM4 Period Register.

Or PWM45 low-byte Period Register

Address 20H: PWM5 Period Register (PWM5PR)

Read/Write-POR		R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x20	PWM5PR	P5PR[7:0]							

Bit[7:0] : P5PR[7:0]

PWM5Period Register.

Or PWM45 high-byte Period Register

5.8 Comparator Register

Address 22H:Comparator Control Register-1 (CMPCON1)

Read/Write-POR		R-x		R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x22	CMPCON1	LVDTSV	-	COUT	CINV	CINS	CM2	CM1	CM0

Bit[7] : LVDTSV

Low Volatge Detect.(4.3/3.6/3.0/2.7V)
= 1 : VDD > 4.3/3.6/3.0/2.7V
= 0 : VDD <= 4.3/3.6/3.0/2.7V

Bit[5] : COUT

Comparator out
CINV = 0:
= 1 : VIN+ > VIN-.
= 0 : VIN+ < VIN-.
CINV = 1:
= 1 : VIN+ < VIN-.
= 0 : VIN+ > VIN-.

Bit[4] : CINV

Output phase selection
= 1 : Inverted output
= 0 : Direct output

Bit[3] : CINS

External input selection
= 1 : PB[3] input
= 0 : PB[4] input

Bit[2:0] :CM[2:0]

Comparator input selection (refer **Figure 4.5-1 comparator diagram)**

CM[2:0]	Description	
	CIN-	CIN+
3'b000	Disable Comparator(sleep mode)	
3'b001	PB[3]	PB[4]
3'b010	CVREF	1V(Bandgap)
3'b011	PB[3]/PB[4]	1V (Bandgap)
3'b100	PB[3]/PB[4]	CVREF
3'b101	TSDCH	VOTP_REF(1V/0.5V)
3'b110,3'b111	Disable Comparator(sleep mode)	

Address 23H: Comparator Control Register-2 (CMPCON2)

Read/Write-POR		R/W-0	-	R/W-0	-	R/W-0	R/W-0	R/W-0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x23	CMPCON2	CVREN	-	CVRR	-	CVR[3:0]			

Bit[7] : CVREN

Reference voltage(CVREF) Enable
=1 : Enable reference voltage CVREF
=0 : Disable reference voltage CVREF

Bit[5] : CVRR

Reference voltage (CVREF) range selection
=1 : Select CVREF low range
=0 : Select CVREF high range

Bit[3:0] :CVR[3:0]

reference voltage(CVREF) .
Set CVRR = 1 :
CV_{REF} = (CVR[3:0]) * Vdd / 18.
Set CVRR = 0 :
CV_{REF} = Vdd / 10 + (CVR[3:0]) * Vdd / 20.

5.9 Temperature Sensor Detect (TSD) Register

Address 21H: Temperature Sensor Detect Control Register(TSDCON)

Read/Write-POR		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x26	TSDCON	NTC1EN	NTC2EN	TSDEN	DTSL[2:0]			VOTPSL[1:0]	

Bit[7:6] : NTC1EN, NTC2EN

Bit[5] : TSDEN

Internal TSDEN Enable
=1 : Enable
=0 : Disable

NTC1EN, NTC2EN, TSDEN	Description
3'b110	Prohibit
3'b100	External **NTC1** Enable
3'b010	External **NTC2** Enable
3'b001	Normal IO , Enable Internal TSDEN
3'b000	Normal IO , Disable Internal TSDEN

Bit[4:2] : DTSL[2:0]

PWM Dead-Time Selection DTSL[2:0]

DTSL[2:0] [2:0]]	Dead Time
3'b000	Disable Dead Time
3'b001	Dead Time 1*Firc clock = 62.5ns
3'b010	Dead Time 2*Firc clock = 125ns
3'b011	Dead Time 4*Firc clock = 250ns
3'b100	Dead Time 8*Firc clock = 500ns
3'b101	Dead Time 16*Firc clock = 1us
3'b110	Dead Time 32*Firc clock = 2us
3'b111	Dead Time 64*Firc clock = 4us

Bit[1:0] : VOTPSL[1:0]

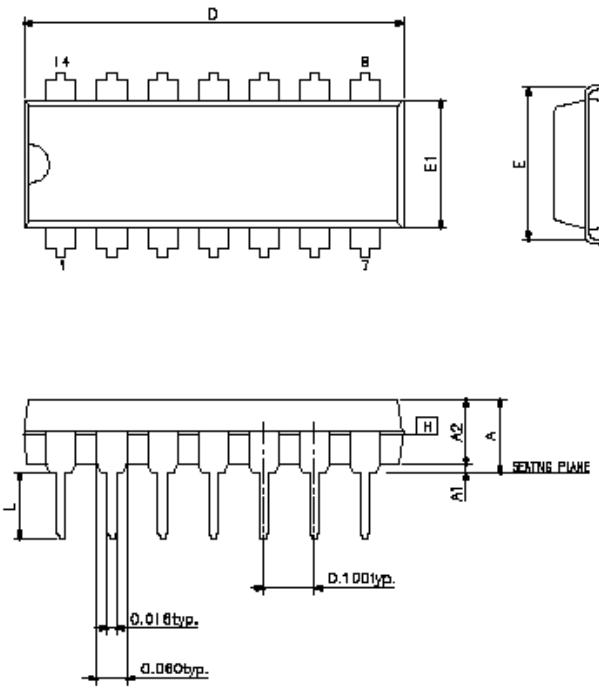
Reference voltage(V_{OTPREF})
=2'b00 : 1V
=2'b01 : 0.5V
=2'b10 : Prohibit
=2'b11 : Prohibit

【6】 Instruction Set

Mnemonic Operands	Description	Cycle	Status Affected
Bit-Oriented	Operations		
BCR R, bit	Clear bit in R	1	-
BSR R, bit	Set bit in R	1	-
BTRSC R, bit	Test bit in R and skip if clear	1/2	-
BTRSS R, bit	Test bit in R and skip if set	1/2	-
Byte-Oriented	& Control Operations		
NOP	No operation	1	-
CLRWDT	Clear Watchdog Timer	1	TO, PD
SLEEP	Go into standby mode	1	TO, PD
(IOST R)	Load R-plane Register	1	-
(IOSTR R)	Read R-plane Register	1	-
RETURN	Return from subroutine	2	-
RETFIE	Return from interrupt, set GIE bit	2	-
CLRA	Clear Acc	1	Z
CLRR R	Clear R	1	Z
MOVAR R	Move Acc to R	1	-
MOVR R, d	Move R	1	Z
COMR R, d	Complement R	1	Z
RRR R, d	Rotate right R	1	C
RLR R, d	Rotate left R	1	C
SWAPR R, d	Swap halves R	1	-
INCR R, d	Increment R	1	Z
INCRSZ R, d	Increment R, Skip if 0	1/2	-
DECR R, d	Decrement R	1	Z
DECRSZ R, d	Decrement R, Skip if 0	1/2	-
ADDAR R, d	Add Acc and R	1	C, DC ,Z
SUBAR R, d	Subtract Acc from R	1	C, DC, Z
ANDAR R, d	AND Acc with R	1	Z
IORAR R, d	Inclusive OR Acc with R	1	Z
XORAR R, d	Exclusive OR Acc with R	1	Z
ADCAR R, d	Add Acc and R with Carry	1	C, DC ,Z
SBCAR R, d	Subtract Acc from R with Carry	1	C, DC ,Z
MOV2 R	Move R to Acc	1	-
Immediate	Data Operations		
MOVIA l	Move immediate to Acc	1	-
ADDIA I	Add Acc with immediate	1	C, DC ,Z
SUBIA I	Subtract Acc from immediate	1	C, DC ,Z
ADCIA I	Add Acc with immediate with Carry	1	C, DC ,Z
SBCIA I	Subtract Acc from immediate with Carry	1	C, DC ,Z
ANDIA I	AND immediate with Acc	1	Z
IORIA l	Inclusive OR immediate with Acc	1	Z
XORIA l	Exclusive OR immediate with Acc	1	Z
RETIA l	Return, place immediate in A	2	-
CALL I	Call subroutine (I : 11 bits)	2	-
GOTO I	Unconditional branch (I : 11 bits)	2	-

【7】 Package Diagram

7-1 14- LEAD (300mil) DIP



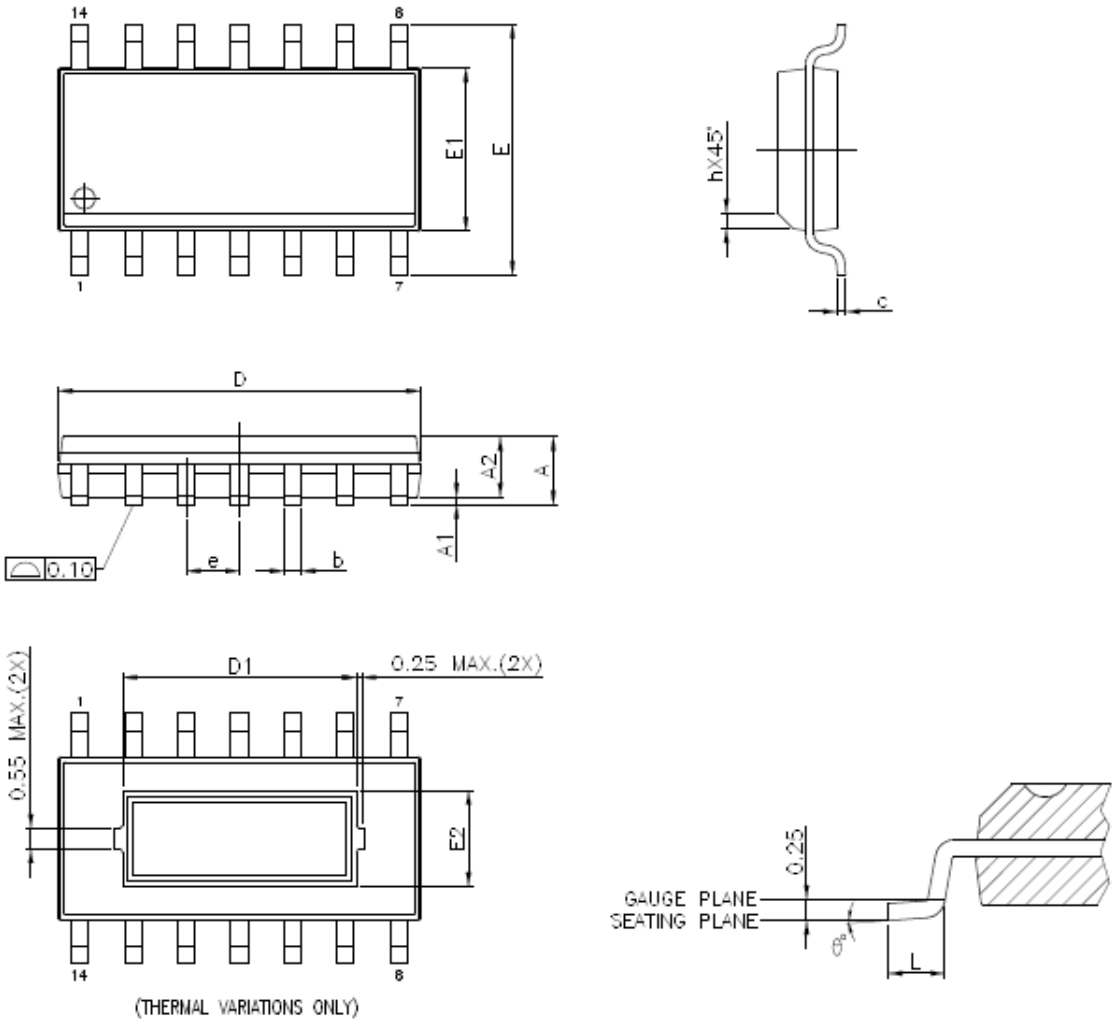
SYMBOLS	MIN.	NOR.	MAX.
A	–	–	0.210
A1	0.015	–	–
A2	0.125	0.130	0.135
D	0.735	0.750	0.775
E		0.300 BSC.	
E1	0.245	0.250	0.255
L	0.115	0.130	0.150
e_B	0.335	0.355	0.375
θ°	0	7	15

UNIT : INCH

NOTES:

1. JEDEC OUTLINE : MS-001 AA
2. "D","E1" DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH.
3. eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
4. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
5. DISTANCE BETWEEN LEADS INCLUDING DAM BAR PROTRUSIONS TO BE .005 INCH MININUM.
6. DATUM PLANE [H] COINCIDENT WITH THE BOTTOM OF LEAD, WHERE LEAD EXITS BODY.

7-2 14- LEAD (150mil) SOP



SYMBOLS	MIN.	MAX.
A	—	1.75
A1	0.10	0.25
A2	1.25	—
b	0.31	0.51
c	0.10	0.25
D	8.65 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
L	0.40	1.27
h	0.25	0.50
θ°	0	8

UNIT : mm

④ THERMALLY ENHANCED DIMENSIONS

PAD SIZE	E2		D1	
	MIN.	MAX.	MIN.	MAX.
10*X23* MIL	1.78	2.44	5.08	5.74

④ "*"表示汎用字元,此汎用字元可能被其它不同字元所取代,
實際的字元請參照bonding diagram所示.
"*" is an universal character, which means maybe replaced by specific character, the actual character please refers to the bonding diagram.

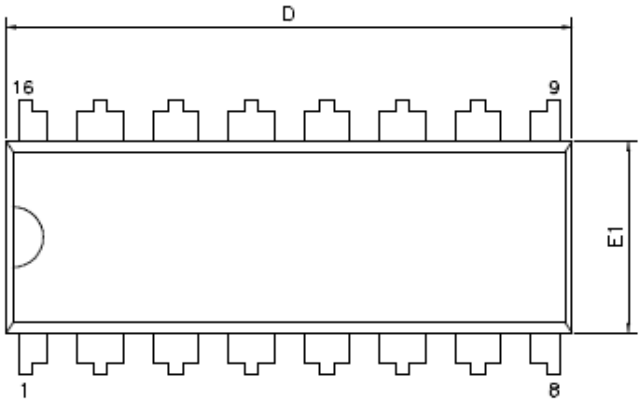
NOTES:

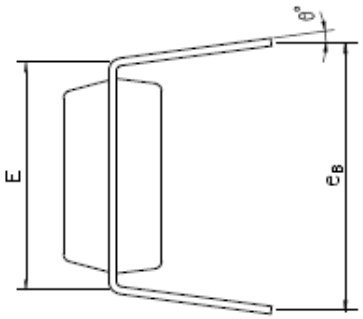
1.JEDEC OUTLINE : MS-012 AB REV.F

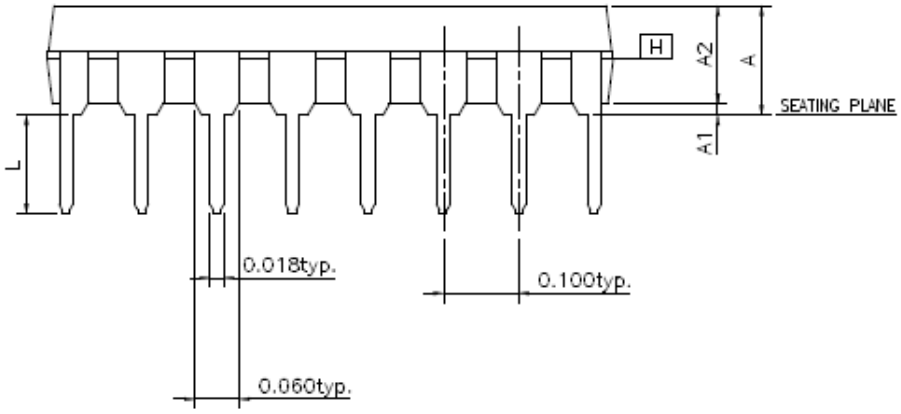
2.DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15mm. PER SIDE.

3.DIMENSIONS "E1" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25mm PER SIDE.

7-3 16- LEAD (300mil) DIP







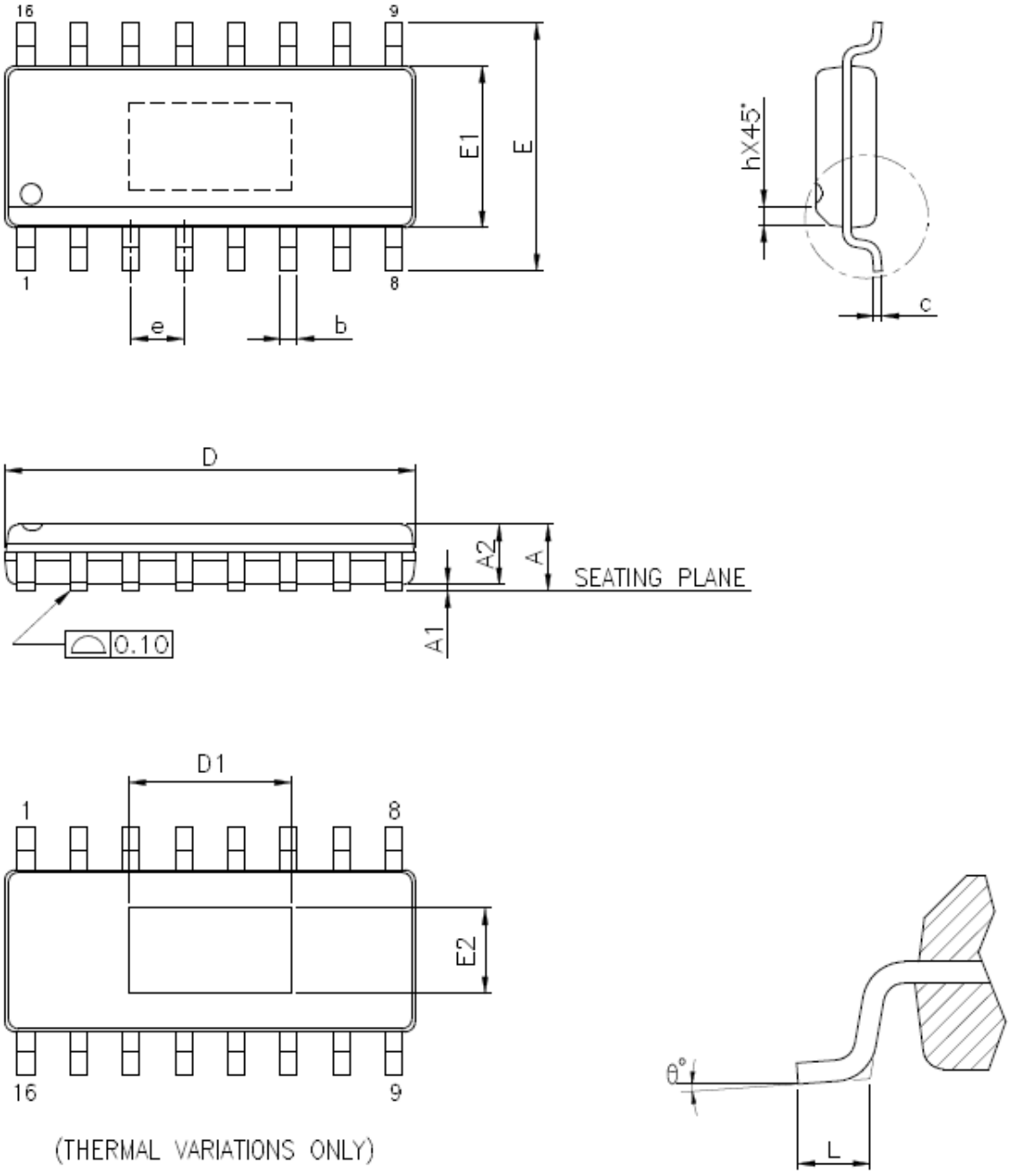
SYMBOLS	MIN.	NOR.	MAX.
A	–	–	0.172
⚠3 A1	0.015	–	0.038
A2	0.125	0.130	0.135
D	0.735	0.755	0.775
E		0.300 BSC.	
E1	0.245	0.250	0.255
L	0.115	0.130	0.150
e_B	0.335	0.355	0.375
$\theta°$	0	7	15

UNIT : INCH

NOTES:

1. JEDEC OUTLINE : MS-001 BB
2. "D","E1" DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH.
3. eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
4. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
5. DISTANCE BETWEEN LEADS INCLUDING DAM BAR PROTRUSIONS TO BE .005 INCH MININUM.
6. DATUM PLANE [H] COINCIDENT WITH THE BOTTOM OF LEAD, WHERE LEAD EXITS BODY.

7-4 16- LEAD (150mil) SOP



	STANDARD		THERMAL	
SYMBOLS	MIN.	MAX.	MIN.	MAX.
A	—	1.75	—	1.70
A1	0.10	0.25	0.00	0.15
A2	1.25	—	1.25	—
b	0.31	0.51	0.31	0.51
c	0.10	0.25	0.10	0.25
D	9.90 BSC		9.90 BSC	
E	6.00 BSC		6.00 BSC	
E1	3.90 BSC		3.90 BSC	
e	1.27 BSC		1.27 BSC	
L	0.40	1.27	0.40	1.27
h	0.25	0.50	0.25	0.50
θ°	0	8	0	8

UNIT : mm

THERMALLY ENHANCED DIMENSIONS(UNIT : mm)

PAD SIZE	E2		D1	
	MIN.	MAX.	MIN.	MAX.
95*X18*	1.68	2.56	3.86	4.72

△7 "*"表示汎用字元,此汎用字元可能被其它不同字元所取代,
實際的字元請參照bonding diagram所示.

△7 "*" is an universal character, which means maybe replaced by specific character, the actual character please refers to the bonding diagram.

NOTES:

1.JEDEC OUTLINE : MS-012 AC REV.F (STANDARD)
MS-012 BC REV.F (THERMAL)

2.DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15mm. PER SIDE.

3.DIMENSIONS "E1" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25mm PER SIDE.