FM8PC712AH

FTC 8-Bit Micro-Controller With 12-bits ADC And CMP

Datasheet R2.2
July 09, 2018

Version Control

Version	Date.	Description
R2.0	2013-12-06	Release of prototype
R2.2	2018-07-09	Add suspend Max current value @P.54

Contents

【1】 FM8PC712AH REVIEW 6
1.1 General Description 6
1.2 Features 6
1.3 Block Diagram 7
1.4 Pin Definitions 7
1.5 Pin Description 8
1.6 Program Memory Mapping 9
1.7 Memory And Register Mapping 9
1.8 Register bit Mapping 10
1.A Table of Optional configuration 12
【2】 Macro-Controller UNIT 13
2.1 Indirect Addressing Define 13
Address 00H : Indirect Addressing Register (INDF) 13
Address 04H :File select Register(FSR) 13
2.2 Program Counter least significant 8 bits 14
Address 02H: Low bytes of Program Counter(PCL) 14
2.3 Status Register 15
Address 03H: Status Register(STATUS) 15
2.4 General Purpose I/O ports 16
2.4.1 PortA, PortB data define 16
Address 05H : Port A(PORTA) 16
Address 06H : Port B(PORTB) 16
2.4.2 PortA, PortB Mode define 17
Address 08H : Port A Mode0 Control Register(PAMODE0) 17
Address 09H : Port A Mode1 Control Register(PAMODE1) 17
Address 0AH : Port b Mode1 Control Register(PBMODE0) 17
Address 0BH : Port B Mode1 Control Register(PBMODE1) 17
2.5 Watchdog Timer(WDT) 19
Address 11h Watchdog Timer(WDT) 19
2.6 Timer0 21
Address 0FH: PWM0 Control Register (TM0CON) 21
Address 0EH: Timer0 value Register (TM0) 22
Address 10H: Timer0 compared or overflow reload byte value Register (TM0RLD) 22

【3】 Power and Reset Management 23
Address 12H : Power Control Register (PCON) 23
【4】 Clock Control 25
Address 13H : Clock configuration (CLKCFG) 25
【5】 System Operating Mode 27
5.1 Overview 27
【6】 PWM Description 30
6.0 PWM/Buzzer Overview 30
6.1 PWM0 Register 32
Address 14H: PWM0 configuration Register(PWM0CON) 32
Address 15H: PWM0 Control Register (PWM0CR) 33
Address 16H: PWM0 Timer Low byte value Register (P0TMLB) 33
Address 17H: PWM0 Timer compared or overflow reload Low byte value Register (P0TMRLDLB) 34
6.2 PWM1 Register 35
Address 20H: PWM1 configuration Register(PWM1CON) 35
Address 21H: PWM1 Control Register (PWM1CR) 36
Address 22H: PWM1 Timer Low byte value Register (P1TMLB) 36
Address 23H: PWM1 Timer compared or overflow reload Low byte value Register (P1TMRLD) 37
6.3 Buzzer Register 37
Address 24H:Buzzer output Select Register(BZS) 37
6.4 PWM Code Example 38
【7】 7+1 Channel Analog to Digital (ADC) 40
7.1 ADC Registers 40
Address 28H: ADC Control _1 Register(ADCON_1) 40
Address 29H: ADC Control_2 Register(ADCON_2) 41
Address 30H: ADC High byte Register(ADCHB) 42
Address 31H: ADC Low byte Register(ADCLB) 42
Address 32H: ADC Control_3 Register(ADCON_3) 42
【8】 Voltage Comparator 43
8.1 CMP Registers 43
Address 35H : Comparator control Register-1(CMPCON1) 43
Address 36H:DAC High byte Register-1(DACR1HB) 45
Address 37H: DAC Low byte Register-1(DACR1LB) 45

Address 38H : Comparator control Register-2(CMPCON2) 46
Address 39H:DAC High byte Register-2(DACR2HB) 46
Address 3AH: DAC Low byte Register-2(DACR2LB) 46
8.2 Comparator with Hysteresis Application 47
【9】 Interrupt 48
9.1 Interrupt Registers 48
Address 0BH : Interrupt Mask Register(INTEN) 48
Address 0CH : Interrupt Flag Register(INTFLAG) 49
Address 0DH : Interrupt Control Register(INTCON) 50
【10】 Instruction Set 51
【11】 Absolute Maximum Ratings 53
【12】 DC Characteristics 53
12.1 General (Operating Temperature = 0 to 70 ℃) 53
12.2 GPIO Interface 55
12.3 ADC specification 56
12.4 CMP specification 56
【13】 Package Diagram 57
13.1 10-PIN MSOP 57

【1】 FM8PC712AH REVIEW

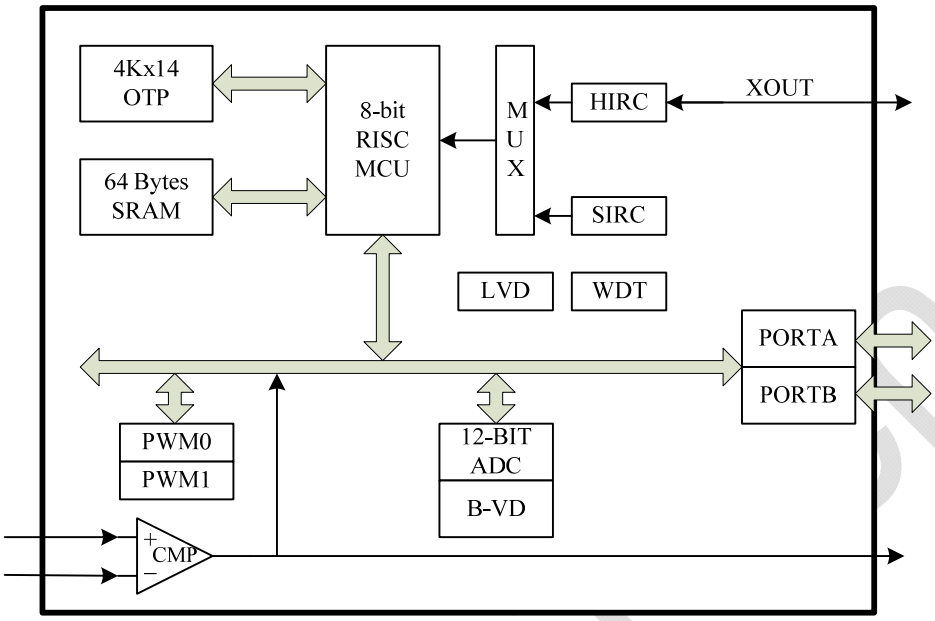
1.1 General Description

- The **FM8PC712AH** is compatible with FM8PC712A.
- The **FM8PC712AH** and FM8PC712A MCU operating frequency are difference.
  - **FM8PC712AH** : VDD > 2.1V → Fcpu ≦ 8Mhz (1T)
  - **FM8PC712A** : VDD > 2.0V → Fcpu ≦ 8Mhz (1T)

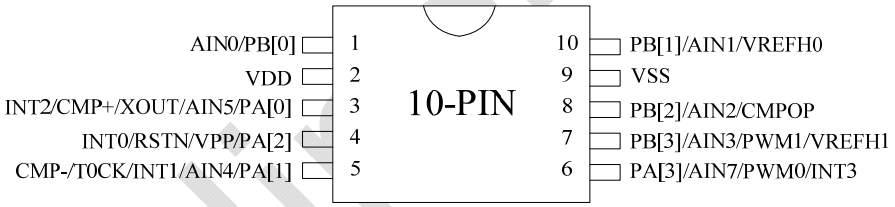
1.2 Features

- **8-bit RISC microprocessor**
  - One clock per instruction cycle (1T).
  - On chip 4.0K x 14 program OTP Memory .
  - 6 level stack.
  - 64 bytes internal SRAM.
  - Optional Firc/(2,4,8,16) MCU clock.
  - One 8-bits Timer , 16-bits(PWM0) and 8-bits (PWM1) counters for PWM output .
  - Watch dog Timer.
- **System Clock**
  - Internal Oscillator
    - Internal 16MHz Oscillator.
    - Internal oscillator 32KHz free run clock for slow/green mode.
- **8 I/O ports**
  - High current drive on any GPIO pin :15mA pin current drive and sink.
  - Each GPIO pin supports high-impedance input, internal pull-ups, open drains output, or CMOS outputs.
- **10 interrupt sources**
  - Four external interrupts is INT0, INT1,INT3,INT4.
  - Six internal interrupts are WDT,Timer0,PWM0,PWM1 ,CMP,ADC;
- **7+1 Channel 12-bit ADC.**
  - Optional Continues or Trigger mode to sample.
  - Support 7 channel external ADC input and a internal VDD/4 ADC input.
  - Build in AD reference voltage (VDD, 4V, 3V, 2V) .
- **Power on Manager**
  - Power on reset (POR) is 2.4V
  - Power down reset (PDR) is 2.0V
  - Three level Low Voltage Detect : LVDH(3.6V),LVDM(3.0V),LVDL(2.4V).
- **Build in PWM(Buzzer) function.**
  - Support two channel PWM .
  - PWM0(Buzzer0)/PWM1(Buzzer1) output pin can be programming.
- **Build in voltage Comparator function.**
  - Low input offset voltage .
  - Build in internal 12-bits DAC comparison voltage .

1.3 Block Diagram



1.4 Pin Definitions

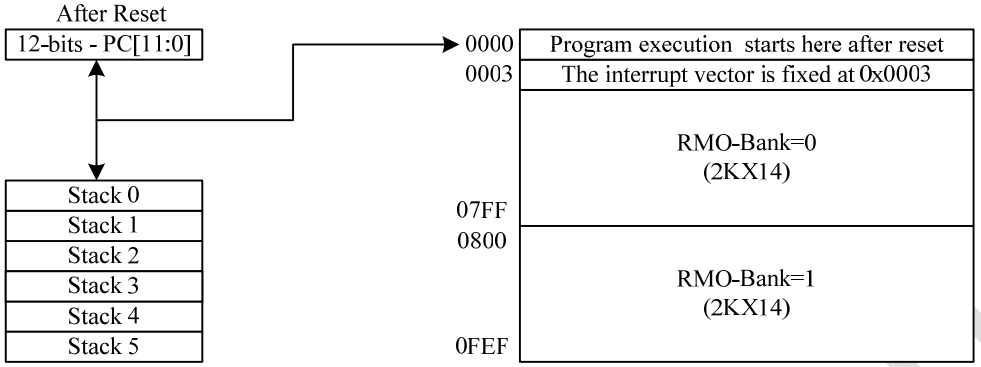


FM8PC712AH
MSOP10

1.5 Pin Description

PIN Name	I/O	10-pin P	-- --	Description
PB[0] AIN0	IO I	1	--	GPIO Port B [0] capable of sinking up to 15mA/pin, or sinking controlled low or high programmable current. Can also source 15 mA drive current or provide a resistive pull-up, or serve as a high-impedance input. ADC input channel-0.
VDD	P	2	--	Power pin.
PA[0] AIN5 CMP+ XOUT INT2	IO I I O	3	--	GPIO Port A [0]capable of sinking up to 15mA/pin, or sinking controlled low or high programmable current. Can also source 15 mA drive current or provide a resistive pull-up, or serve as a high-impedance input. ADC input channel-5. Positive input of comparator Up to 16Mhz ceramic resonator or external clock output when external Crystal enable. External interrupt input , falling edge or pin change trigger.(low-current)
PA[1] CMP- AIN4 T0CK INT1	IO I I I I	5	--	GPIO Port A [1]capable of sinking up to 15mA/pin, or sinking controlled low or high programmable current. Can also source 15 mA drive current or provide a resistive pull-up, or serve as a high-impedance input. Negative input of comparator ADC input channel-4. External clock for PWM0 External interrupt input , falling edge or pin change trigger.(low-current)
PA[2] VPP RSTN INT0	I/O I I I	4	--	GPIO Port A [2] input/output and a resistive pull-up(normal). Programming voltage supply, VCC for normal operation Only F/W can set to External reset pin . It's active low. External interrupt input , falling edge trigger. (low-current)
PA[3] PWM0 AIN7 INT3	IO O I	6	--	GPIO Port A [3] capable of sinking up to 15mA/pin, or sinking controlled low or high programmable current. Can also source 15 mA drive current or provide a resistive pull-up, or serve as a high-impedance input. The power on is pull-high 100K ohm to VDD. PWM0 signal output pin when PWM0 enable. External interrupt input , falling edge or pin change trigger.(low-current)
PB[3] VREFH1 AIN3 PWM1	IO I O	7	--	GPIO Port B [3] capable of sinking up to 15mA/pin, or sinking controlled low or high programmable current. Can also source 15 mA drive current or provide a resistive pull-up, or serve as a high-impedance input. External high reference 1 voltage input of ADC ADC input channel-3. PWM1 signal output pin when PWM1 enable.
PB[2] CMPOP AIN2	IO O I	8	--	GPIO Port B [2] capable of sinking up to 15mA/pin, or sinking controlled low or high programmable current. Can also source 15 mA drive current or provide a resistive pull-up, or serve as a high-impedance input. Output of comparator ADC input channel-2.
VSS	G	9	--	Ground
PB[1] AIN1 VREFH0	IO I	10	--	GPIO Port B [1] capable of sinking up to 15mA/pin, or sinking controlled low or high programmable current. Can also source 15 mA drive current or provide a resistive pull-up, or serve as a high-impedance input. ADC input channel-1. External high reference 0 voltage input of ADC

1.6 Program Memory Mapping



(Address : 0FF0~0FFF Revered for Configuration)

1.7 Memory And Register Mapping

Table 1.7-1 I/O Register Mapping

Address	Description(F-plane)	Address	R-Plane
00h	INDF		
01h	--		
02h	PCL		
03h	STATUS		
04h	FSR		
05h	PORTA		
06h	PORTB		
07h	--(Revered)		
08h	--(Revered)	08h	*PAMODE0
09h	--(Revered)	09h	*PAMODE1
0Ah	--(Revered)	0Ah	*PBMODE0
0Bh	INTEN	0Bh	*PBMODE1
0Ch	INTFLAG		
0Dh	INTCON		
0Eh	TM0		
0Fh	TM0CON		
10h	T0RLD		
11h	WDT		
12h	PCON		
13h	CLKCFG		
14h	PWM0CON		
15h	PWM0CR		
16h	P0TMLB		
17h	P0TMRLDLB		
18h	P0TMHB		
19h	P0RDHB		
20h	PWM1CON		
21h	PWM1CR		
22h	P1TM		
23h	P1TMRD		
24h	Buzzer		
25h~27h	Revered		
28h	ADCON_1		
29h	ADCON_2		

Address	Description(F-plane)	Address	R-Plane
30h	ADCHB		
31h	ADCLB		
32h	ADCON_3		
33~34	Revered		
35h	CMPCON1		
36h	DACR1HB		
37h	DACR1LB		
38h	CMPCON2		
39h	DACR2HB		
3Ah	DACR2LB		
3B~3F	(Revered)		
40h | 7Fh	SRAM 64 bytes		

*Accessed by IOST/IOSTR instruction
*The R-plane Registers are loaded with the contents of the ACC register by executing the IOST instruction. By executing the IOSTR instruction, user read these registers

1.8 Register bit Mapping

TABLE 1.7-2: Operational Registers Map

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
00h (R/W)	INDF	Uses contents of FSR to address data memory(not a physical register)							
01h (R/W)	Revered	--							
02h (R/W)	PCL	Low order 8 bits of PC							
03h (R/W)	STATUS	--	ROMBK	FRP	/TO	/PD	Z	DC	C
04h (R/W)	FSR	--	Indirect data memory address pointer						
05h (R/W)	PORTA	--	--	--	--	PORTA[3]	PORTA[2]	PORTA[1]	PORTA[0]
06h (R/W)	PORTB	--	--	--	--	PORTB[3]	PORTB[2]	PORTB[2]	PORTB[0]
07h	Revered	--	--	--	--	--	--	--	--
08h	Revered	--	--	--	--	--	--	--	--
09h	Revered	--	--			--	--	--	--
0Ah	Revered								
0BH(R/W)	INTEN	GIE	--	--	INT3IE	INT2IE	INT1IE	INT0IE	TM0IE
0Ch (R/W)	INTFLAG	--	--	--	INT3IF	INT12IF	INT1IF	INT0IF	TM0IF
0Dh(R/W)	INTCON	SELINT1[2:0]			INT3CON	INT2CON	INT1CON	INT0CON	--
0Eh(R/W)	TM0	TM0[7:0] 8-bit real time clock/counter							
0Fh(R/W)	TM0CON	TM0EN	--	TM0PS[2:0]			TM0CKS[2:0]		
10h(R/W)	TM0RLD	TM0RLD[7:0]							
11h(R/W)	WDT	WDTE	WDTSL	WDTPS2	WDTPS1	WDTPS0	LVRSL	SPSEL	--
12h(R/W)	PCON	--	GRN_MD	LVDIS	RSTSL1	RSTSL0	LVDT36	LVDT24	LVDT30
13h(R/W)	CLKCFG	SELCLK2	SELCLK1	SELCLK0	CLKSW	ATSW	INCODS	EXOSEN	IRCEN
14h(R/W)	PWM0CON	P0INTSL	P0DT2	P0DT1	P0DT0	P0CKS1	P0CKS0	P0OSEL[1:0]	
15h(R/W)	PWM0CR	PWM0E	P0OUTS	P0TPS2	P0TPS1	P0TPS0	P0TMEN	P0TMIE	P0TMIF
16h(R)	P0TMLB	P0TM[7:0]							
17h(R/W)	P0TMRLDLB	P0TMRLD[7:0]							
18h(R)	P0TMHB	P0TM[15:8]							
19h(R/W)	P0TMRLDHB	P0TMRLD[15:8]							
20h(R/W)	PWM1CON	P1INTSL	P1DT2	P1DT1	P1DT0	P1CKS1	P1CKS0	P1OSEL[1:0]	

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
21h(R/W)	PWM1CR	PWM1E	P1OUTS	P1TPS2	P1TPS1	P1TPS0	P1TMEN	P1TMIE	P1TMIF
22h(R/W)	P1TM	P1TM[7:0]							
23h(R/W)	P1TMRLD	P1TMRLD[7:0]							
24h	Buzzer	BZS1	BZS0	Revered	Revered	Revered	Revered	Revered	Revered
25~27h	Revered	Revered	Revered	Revered	Revered	Revered	Revered	Revered	Revered
28h(R/W)	ADCON_1	ADCEN	ADCST	CHSEL[2:0]			--	ADCSR[1:0]	
29h(R/W)	ADCON_2	ADCIE	ADCIF	SVERFH	ADCNT	SELH	ADCTMS	SELVER1	SELVER0
30h(R)	ADCHB	ADCB[11]	ADCB[10]	ADCB[9]	ADCB[8]	ADCB[7]	ADCB[6]	ADCB[5]	ADCB[4]
31h(R)	ADCLB	--	--	--	--	ADCB[3]	ADCB[2]	ADCB[1]	ADCB[0]
32h(R/W)	ADCOM_3	INEN[7]	--	INEN[5]	INEN[4]	INEN[3]	INEN[2]	INEN[1]	INEN[0]
35h(R/W)	CMPCON1	CMPEN	COP1	CMPIE1	CMPRIF1	CMPFIF1	CMPMD[2:0]		
36h(R/W)	DACR1HB	DACR1[11:4]							
37(R/W)	DACR1LB	--	--	--	--	DACR1[3:0]			
38h(R/W)	CMPCON2	CMPINT1	COP2	CMPIE2	CMPRIF2	CMPFIF2	CMPINT2	TOGSEL	--
39h(R/W)	DACR2HB	DACR2[11:4]							
3Ah(R/W)	DACR2LB	--	--	--	--	DACR2[3:0]			

Legend: - = unimplemented, read as '0',

1.A Table of Optional configuration

<table>
<tr><th>Config Name</th><th>Description</th><th>Default</th></tr>
<tr><td>SELXOUT[1:0]</td><td>Select IRC output Clock
<table>
<tr><td>SLEXOUT [1:0]</td><td>Freaquency</td></tr>
<tr><td>2’b11</td><td>Firc = 16Mhz</td></tr>
<tr><td>2’b10</td><td>Firc/2 = 8Mhz</td></tr>
<tr><td>2’b01</td><td>Firc/4 = 4Mhz</td></tr>
<tr><td>2’b00</td><td>Firc /8 = 2Mhz</td></tr>
</table></td><td>2b11</td></tr>
<tr><td>SelCpuClk[2:0]</td><td>Select Fcpu clock
<table>
<tr><td>SelCpuClk[2:0]</td><td>Fcpu</td></tr>
<tr><td>3’b111</td><td>1MHz</td></tr>
<tr><td>3’b011</td><td>2MHz</td></tr>
<tr><td>3’b010</td><td>4MHz</td></tr>
<tr><td>--</td><td>--</td></tr>
<tr><td>--</td><td>--</td></tr>
</table></td><td>3’b111</td></tr>
<tr><td>INSWDY</td><td>Internal clock switch to external clock delay time
1 = 128us delay
0 = 4ms delay</td><td>1’b1</td></tr>
<tr><td>WDTSEL</td><td>Watch dog time out select
WDTSEL[1:0] : 2’b00 = 128 ms
2’b01 = 512 ms
2’b10 = 8 ms
2’b11 = 32 ms</td><td>2’b11</td></tr>
<tr><td>selPor</td><td>Power on reset extend timing
SelPor[1:0] : 2’b00 = 8 ms
2’b01 = 16 ms
2’b10 = 32 ms
2’b11 = 64 ms</td><td>11</td></tr>
<tr><td>PROTECT</td><td>1: No protect ROM code

0: Protect ROM code</td><td>1→ no protect</td></tr>
</table>

【2】 Macro-Controller UNIT

2.1 Indirect Addressing Define

The INDF Register is not a physical register .Any instruction accessing the INDF register can actually access the register pointed by FSR Register. Reading the INDF register itself indirectly(FSR="0") will read 0x00.Writing to the INDF register indirectly results in a no-operation.
The bits 6~0 of FSR register can be select up to 128 registers by accessed.(address 00~7fh).

Address 00H : Indirect Addressing Register (INDF)

Bits	7	6	5	4	3	2	1	0
Name	Uses contents of FSR to address data memory							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Address 04H :File select Register(FSR)

Bits	7	6	5	4	3	2	1	0
Name	File select register to define address in indirect addressing mode only 7 bits							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Example : How to used instruction at Indirect addressing
(1) Write AA data to Register (address=8'h50h)

```
MOVIA    7Fh
MOVAR    FSR        ;  Register address pointer is 7Fh
MOVIA    AAh
MOVAR    INDF       ; Move  data = AAh to address = 7Fh register
```

(2)Read register(50h) to ACC

```
MOVIA    7Fh
MOVAR    FSR        ;  Register address pointer is 7Fh
MOVR     INDF,A     ; Move  contents of register(7Fh) to ACC
```

2.2 Program Counter least significant 8 bits

A special computed GOTO is accomplished by adding an offset to the program counter (ADDAR PCR,R). When doing a table read using this method, care should be taken if the table location crosses a PCL memory boundary(256 word block).

Address 02H: Low bytes of Program Counter(PCL)

Bits	7	6	5	4	3	2	1	0
Name	Uses contents of FSR to address data memory							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Example : Create table

```
            MOVR   TABLECNT,A
             CALL     TABLE1
              .
              .
TABLE1    : ADDAR    PCL,R          ;  PCL = TABLECNT
             RETIA      00h          ; TABLECNT=0
             RETIA      01H          ; TABLECNT=1
             RETIA      02H          ; TABLECNT=2
             RETIA      02H          ; TABLECNT=3
```

2.3 Status Register

This register contains the arithmetic status of the ALU, the RESET status.
If the STAUTS Register the destination for an instruction the affects the Z,DC or C bits, then the write to these three bits disabled. These bits are set or cleared according to the logic. Furthermore, the /TO and /PD bits are not writable.

Address 03H: Status Register(STATUS)

Bits	7	6	5	4	3	2	1	0
Name	Revered	ROMBK	FRP	/TO	/PD	Z	DC	C
Read/Write	R	R/W	R/W	R	R	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[6] : ROMBK
1 : select Program ROM is Bank 1.(PC=0x800~0xFEF)
0 : select Program ROM is Bank 0.(PC=0x000~0x7FF)

Bit[5] : FRP
1: When BSR/BCR instruction execute, the other bit of GPIO(PA/PB) updated from PIN(PA/PB)
0: When BSR/BCR instruction execute, the other bit of GPIO(PA/PB) updated from register (PA/PB register)

Bit[4] : /TO
WDT overflow flag bit.
1 = After power on or by the CLRWDT or SLEEP instruction.
0 = A watch-dog time overflow.

Bit[3] : /PD
Power down flag flag.
1 = After power on or by the CLRWDT instruction.
0 = By the SLEEP instruction.

Bit[2] : Z
Zero flag
1 = The result of a logic operation is zero.
0 = The result of a logic operation is not zero.

Bit[1] : DC
Auxiliary carry flag or borrow flag
ADDAR, ADDIA
1 = A carry from the 4th low order bit of the result occurred.
0 = A carry from the 4th low order bit of the result did not occurred.
SUBAR,SUBIA
1 = A borrow from the 4th low order bit of the result did not occurred.
0 = A borrow from the 4th low order bit of the result occurred.

Bit[0] : C
Carry flag or borrow flag.
ADDAR, ADDIA, RLR
1 = A carry occurred.
0 = A Carry did not occurred.
SUBAR, ADDIA, RRR
1 = A borrow did not occurred.
0 = A borrow occurred.

2.4 General Purpose I/O ports

Ports A are 8 bits I/O register. Ports B are 4 bits I/O register ,each bit can also selected as an external interrupt source for the microcontroller.
***Figure* 2-4.1** shows a diagram of a GPIO port pin.
Refer **TABLE 2.4.3-1**, each pin can be independently configured as high-impedance inputs, inputs with internal pull-ups, open drain outputs, or traditional output s with selectable drive strength.
After reset, all GPIO data and controlled mode register is cleared, so the GPIO pins are as input mode.

2.4.1 PortA, PortB data define

Address 05H : Port A(PORTA)

Bits	7	6	5	4	3	2	1	0
Name	--	--	--	--	PORTA[3]	PORTA[2]	PORTA[1]	PORTA[0]
Read/Write	--	--	--	--	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7:0]: PORTA[3:0] data input/Ouput
1 = Port pin is logic HIGH
0 = Port pin is logic LOW

Address 06H : Port B(PORTB)

Bits	7	6	5	4	3	2	1	0
Name	--	--	--	--	PORTB[3]	PORTB[2]	PORTB[1]	PORTB[0]
Read/Write	--	--	--	--	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7:0]: PORTB[3:0] data input/Ouput
1 = Port pin is logic HIGH
0 = Port pin is logic LOW

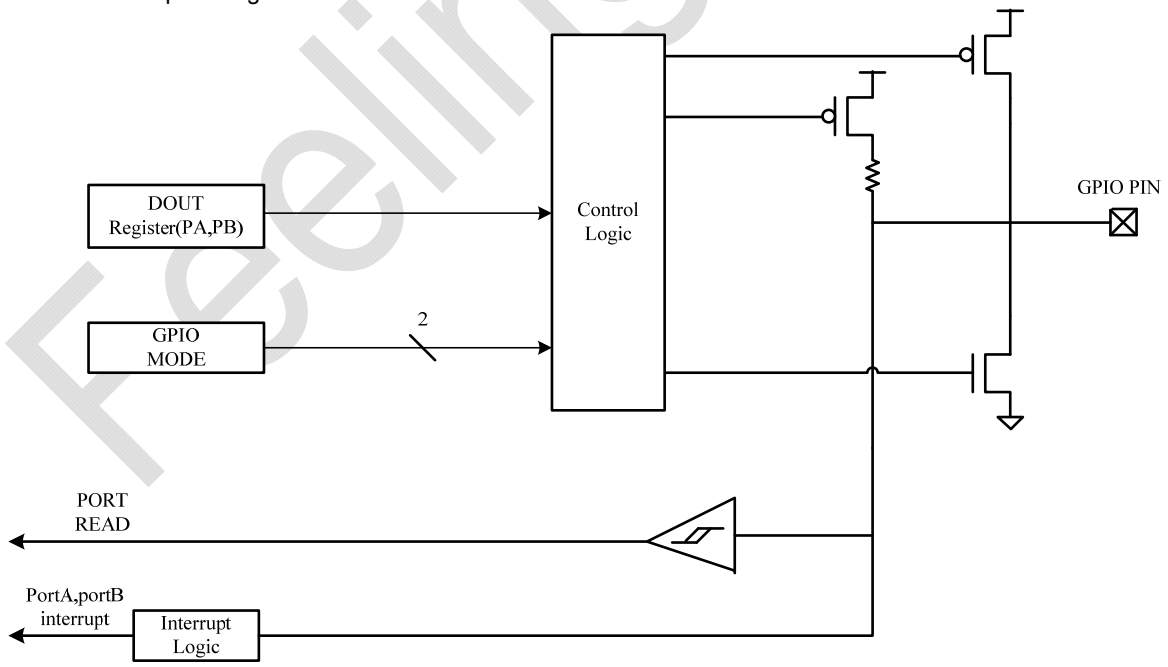


Figure 2.4-1 Block diagram of GPIO Port

2.4.2 PortA, PortB Mode define

Address 08H : Port A Mode0 Control Register(PAMODE0)

Bits	7	6	5	4	3	2	1	0
Name	--	--	--	--	PAMD0[3:0]			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	1	1	0	0

Accessed by IOST/IOSTR instruction

Bit[7:0] : PAMD0[3:0]
1 = Port pin Mode 0 is logic HIGH
0 = Port pin Mode 0 is logic LOW

Address 09H : Port A Mode1 Control Register(PAMODE1)

Bits	7	6	5	4	3	2	1	0
Name	--	--	--	--	PAMD1[3:0]			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Accessed by IOST/IOSTR instruction

Bit[7:0] : PA [3:0] Mode 1
1 = Port pin Mode 1 is logic HIGH
0 = Port pin Mode 1 is logic LOW

Note : PA[2] (VPP) : Default is pull high 100K and External Reset
PA[3] : Default is pull high 100K;

Address 0AH : Port b Mode1 Control Register(PBMODE0)

Bits	7	6	5	4	3	2	1	0
Name	--	--	--	--	PBMD1[3:0]			
Read/Write	--	--	--	--	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Accessed by IOST/IOSTR instruction

Bit[7:0] : PBMD0[3:0]
1 = Port pin Mode 0 is logic HIGH
0 = Port pin Mode 0 is logic LOW

Address 0BH : Port B Mode1 Control Register(PBMODE1)

Bits	7	6	5	4	3	2	1	0
Name	--	--	--	--	PBMD1[3:0]			
Read/Write	--	--	--	--	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

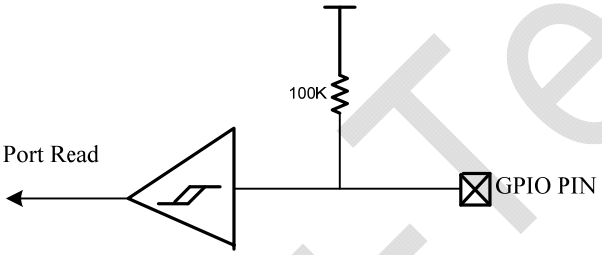
Accessed by IOST/IOSTR instruction

Bit[7:0] : PBMD1[3:0]
1 = Port pin Mode 1 is logic HIGH
0 = Port pin Mode 1 is logic LOW

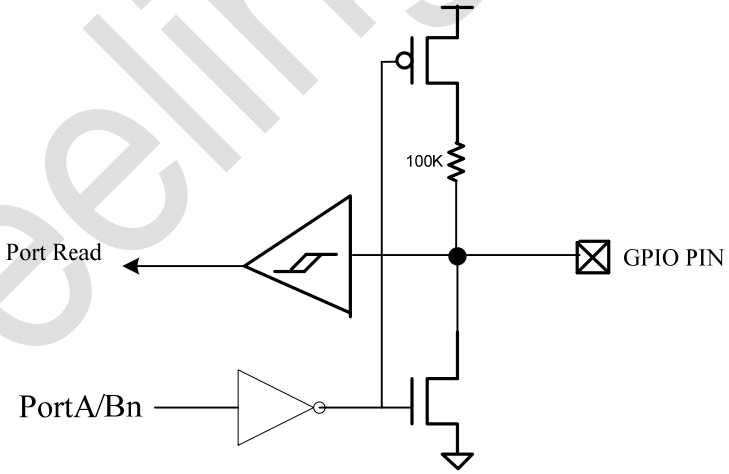
Each pin of PORTA,PORTB mode is define by as follows **TABLE 2.4.3-1 :**

TABLE 2.4.3-1 Port A and B Output control truth Table

Data register	Mode1	Mode0	Output Drive Strength
1 0	0	0	HI-z(Input mode)
1 0	0	1	Pull-High(input mode)
1	1	0	Resistive(100KΩ)
0			Sink (15mA)
1	1	1	Normal Drive(15mA)
0			Sink (15mA)



Mode1=0 and Mode0=1 Pull-High(input mode)



Mode1=1 and Mode0=0 Open-Drain Mode

2.5 Watchdog Timer(WDT)

The Watchdog Timer (WDT) is a free running on chip RC oscillator which dose not require any external components. So the WDT will still run into SLEEP mode. During normal operation or in SLEEP mode, a WDT time-out will cause base on Configuration option to the device reset .

Configuration WDTSEL[1:0]	VDD=5V~2.4vV SIRC = 32Khz,WDT Time out
2'b11	32 ms
2'b10	8 ms
2'b01	512 ms
2'b00	128 ms

The CLRWDT instruction clears the WDT , if assigned to the WDT, and prevents it from timing out and generating a device reset.
The WDT can be disabled by clearing the control bit WDTE(08h-7). The WDT has a normal time-out period of 18ms(without precaler). When the SLEEP instruction executes , the MCU will be reset or go next instruction on WDT time-out.
The prescaler of WDT refers **Table2.5-1**.
The block diagram of WDT shows in ***Figure* 2.5-2**.

Address 11h Watchdog Timer(WDT)

Bits	7	6	5	4	3	2	1	0
Name	WDTE	WDTSL	WDTPS[2:0]			LVRSL	SPSEL	--
Read/Write	R/W	R/W	R/W			R/W	R/W	--
Default	1	1	0	0	0	0	1	0

Bit[7] : WDTE
Watch-Dog timer enable.
1 = Enable.
0 = Disable.
Bit[6] : WDTSL
Watch-dog timer out select .
1 = If Watch-dog timer out ,the Device be reset.(PC = 0x0000h)
0 = If Watch-dog timer out ,Device be wake up and PC = PC+1.

Bit[5:3] : WDTPS[2:0]
WDT Prescaler, Please refer **Table 2.5-1**.

WDTPS[2:0]	WDT time out(config = 32ms)
3'b000	32ms*1 = 32 ms
3'b001	32ms*2 = 64 ms
3'b010	32ms *4 = 128 ms
3'b011	32ms *8 = 256 ms
3'b100	32ms *16 = 512 ms
3'b101	32ms *32 = 1024 ms
3'b110	32ms *64 = 2048 ms
3'b111	32ms *128 = 4096 ms

TABLE 2.6-1 WDT Prescaler

Bit[2] : LVRSL
LVR select .
1 = When Device is in green mode , the LVR signal can wake up to normal mode(PC=PC+1) .
0 = When Device is in green mode , the LVR signal will be reset chip. (PC=0000h) .

Bit][1] : SPSEL

Slow IRC clock selection

1 : Slow IRC Clock don't vary with VDD
0 : Slow IRC Clock vary with VDD

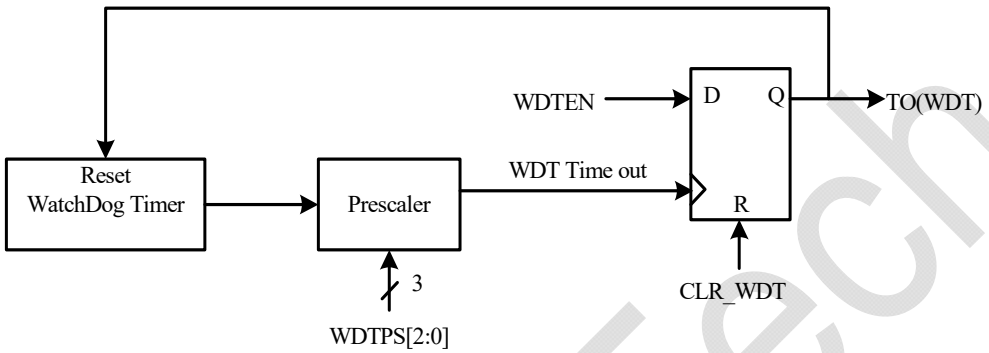


Figure **2.5-2 Block Diagram of WDT**

2.6 Timer0

The Timer0 is a 8 bits Timer/Counter . The Timer0 can operate as either a timer or an interrupt event counter. The The Timer0 block diagram is as show in Figure 2.6-1.

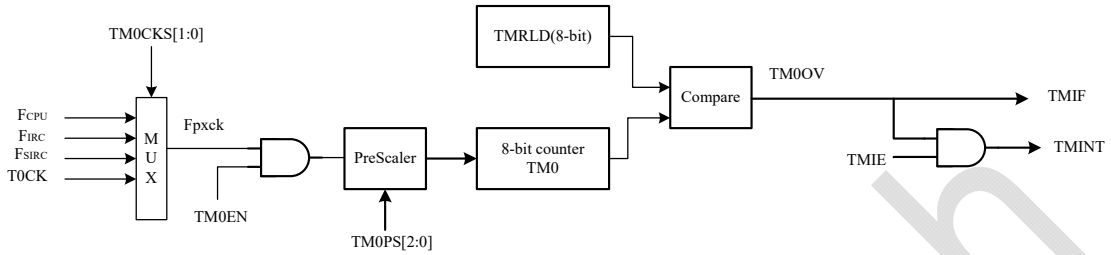


Figure 2.6-1 Block Diagram of Timer0

Address 0FH: PWM0 Control Register (TM0CON)

Bits	7	6	5	4	3	2	1	0
Name	TM0EN	--	TM0PS[2:0]			TM0CKS[1:0]		--
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7] :TM0EN

TM0 module enable.
1 = Enable.
0 = Disable.

Bit[6] : Revered

Bit[5:3] : TM0PS[2:0]

TM0 Timer prescaler, as follow Table 8-4:

TM0PS [2:0]	TM0 MODE
3'b000	TM0 Timer clock select is FT0ck /2
3'b001	TM0 Timer clock select is FT0ck /4
3'b010	TM0 Timer clock select is FT0ck /8
3'b011	TM0 Timer clock select is FT0ck /16
3'b100	TM0 Timer clock select is FT0ck /32
3'b101	TM0 Timer clock select is FT0ck /64
3'b110	TM0 Timer clock select is FT0ck /128
3'b111	TM0 Timer clock select is FT0ck /256

Table 8-4 PWM0 Timer clock select

Bit[2:1] :TM0CKS[1:0]

TM0 Timer clock select.

TM0CKS[1:0]	Clock select (FT0ck)
2'b00	FCPU
2'b01	FIRC (16Mhz)
2'b10	Fsirc
2'b11	T0CK(External clock)

Address 0EH: Timer0 value Register (TM0)

Bits	7	6	5	4	3	2	1	0
Name	P0TM[7:0]							
Read/Write	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bit[7:0] : TM0[7:0]
Timer 0 counter value.

Address 10H: Timer0 compared or overflow reload byte value Register (TM0RLD)

Bits	7	6	5	4	3	2	1	0
Name	TM0RLD[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7:0] : TM0RLD[7:0]
Timer0 compared or overflow reload byte

【3】 Power and Reset Management

There are Four cases of reset on USB controller chip. These cases of reset occurrence are listed below.

1. Power On/down Reset (normal mode)
   - ◆ POR (VDD ≤ 2.4V) and PDR (VDD ≤ 2.0V)
2. Brown out reset
   - ◆ LVDT24 (VDD ≤ VLVR1 ==2.4V for > 100ns)
   - ◆ LVDT30 (VDD ≤ VLVR2 ==3.0V for > 100ns)
   - ◆ LVDT36 (VDD ≤ VLVR2 ==3.6V for > 100ns)
3. Watchdog Reset
   - ◆ WDR (Watch Dog time out)
4. External Reset(PA[2])
   - ◆ EXTR (Low active)
5. Power down Reset (sleep mode)
   - ◆ PDRS (VDD ≤ 1.3V)

If the POR,PDR,PDRS,WDR, LVDT24 , LVDT3.0 or EXTR occurs, the chip will enter reset status. The following events take place on reset status.
All registers are reset to their default values expect status registers.
The status register (03h) is reset to their default value only for POR/PDR/PDRS .
After reset status, program counter begins at address 0x0000.
PORN is asserted when VDD voltage to the device is upper approximately 2.4V(see *Figure* 3.0-1).

Address 12H : Power Control Register (PCON)

Bits	7	6	5	4	3	2	1	0
Name	Revered	GREEN_MD	LVDIS	RSTSL[1:0]		LVDT36	LVDT24	LVDT30
Read/Write	R	R/W	R/W	R/W	R/W	R	R	R
Default	0	0	0	0	0	0	0	0

Bit][7] : Revered

.

Bit][6:5] : GREEN_MD,LVDIS

{ GREEN_MD,LVDIS}	Description
2'b00	Normal Mode, and All LVD36,LVDT30,LVDT24 circuit are enable
2'b01	First switch Fcpu clock is Fsirc. Slow Mode, and All LVD36,LVDT30,LVDT24 circuit are disable Fcpu enable(Fcpu = Fsirc),
2'b10	Green Mode , and All LVD36,LVDT30,LVDT24 circuit are enable Fcpu Disable.
2'b11	Green Mode , and All LVD36,LVDT30,LVDT24 circuit are disable Fcpu Disable.

Bit[4:3] : RSTSL[1:0]*

RSTSL[1:0]	Description
2'b00	POR,PDR,PDRS,WDR can reset system chip.
2'b01	POR,PDR,PDRS,WDR, LVDT30 (VDD<= 3.0V) can reset system chip
2'b10	POR, PDR,PDRS ,WDR ,LVDT24 (VDD<= 2.4V) can reset system chip
2'b11	POR, PDR,PDRS ,WDR ,EXR(PA[2]) can reset system chip.

*POR,PDR,PDRS occurs, the **RSTSL[1:0]** can be reset to default value.
*WDR, LVDT24 , LVDT3.0 or EXR occurs, the **RSTSL[1:0]** can't be reset to default value.

Bit[2] : LVDT36 (Read only)
Low Voltage(3.6V) detect signal.
1 = VDD voltage > 3.6V. ; 0 = VDD voltage <= 3.6 V

Bit[1] : LVDT24

Low Voltage(2.4V) detect signal.
1 = VDD voltage > 2.4V.
0 = VDD voltage <= 2.4 V

Bit[0] : LVDT30

Low Voltage(3.0V) detect signal.
1 = VDD voltage > 3.0V.
0 = VDD voltage <= 3.0 V

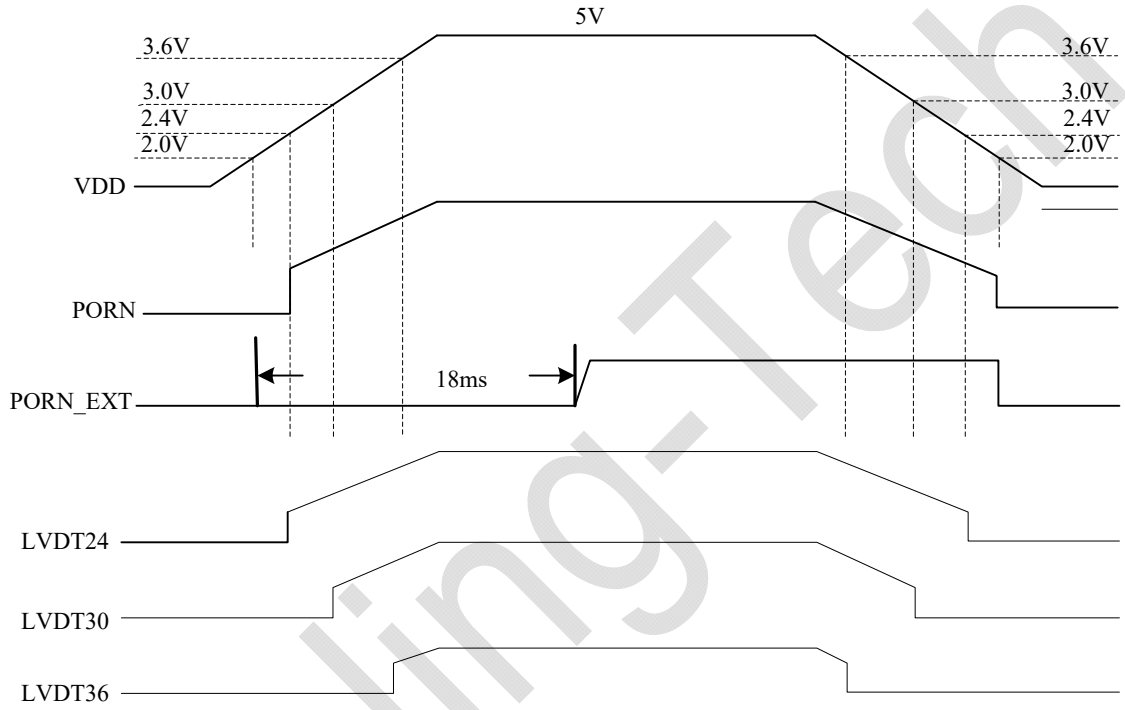


Figure 3.0-1 Power on Reset and LVD24,LVDT30,LVDT36 Timing

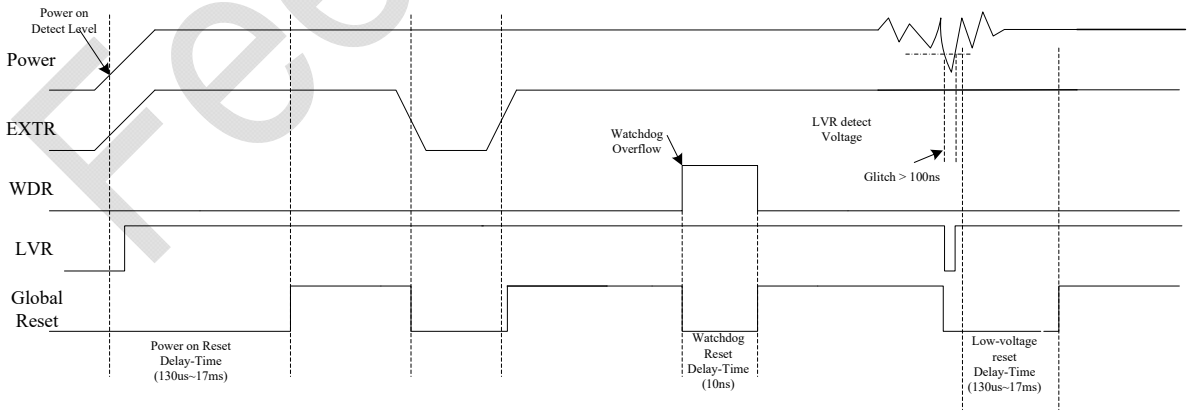


Figure 3.0-2 Global Timing

【4】 Clock Control

The MCU operation frequency rang is as following : (Fcpu is MCU clock)
(1) VDD > 2.1V → Fcpu ≦ 8Mhz (1T)

Address 13H : Clock configuration (CLKCFG)

Bits	7	6	5	4	3	2	1	0
Name	SELCLK[2:0]			CLKSW	ATSW	INCODS	EXOSEN	IRCEN
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	1	1	0	1

Bit[7:5] : SELCLK[2:0]
Select MCU switch-clock .(FIRC=16Mhz)

SELCLK[2:0]	Select clock(Fsel) EXOSEN=0	Select clock(Fsel) EXOSEN=1
3'b000	(FIRC)/4 = 4Mhz	T0CK/4
3'b001	(FIRC)/16 = 1Mhz	T0CK/16
3'b010	(FIRC)/8 = 2Mhz	T0CK/8
3'b011	(FIRC)/2 = 8Mhz	T0CK/2
3'b100	---	
3'b101	FSIRC	FSIRC

Bit[4] : CLKSW
CPU clock switch
1 = CPU clock start to switch from Ffig clock to Fsel clock.
0 = CPU clock start to switch from Fsel clock to Ffig clock.

Bit[3] : ATSW
Enable auto switch clock
1 = Enable auto clock switch Fcpu to 4Mhz clock when VDD < 3.0V
0 = Disable auto clock switch Fcpu to 4Mhz clock when VDD < 3.0V

Bit[2] : INCODS
Internal clock output disable.
1 = Disable internal IRC clock output.
0 = Enable internal IRC clock output. The IRC clock is driven output to XOUT pin.

Bit[1] : EXOSEN
External Oscillator Enable.
1 = Enable the external oscillator . The Fcpu clock is switch to external clock(Fosc) from FIRC clock.
0 = Disable Oscillator Enable.

Bit[0] : IRCEN
Internal clock enable.
1 = Enable internal clock
0 = Disable internal clock.

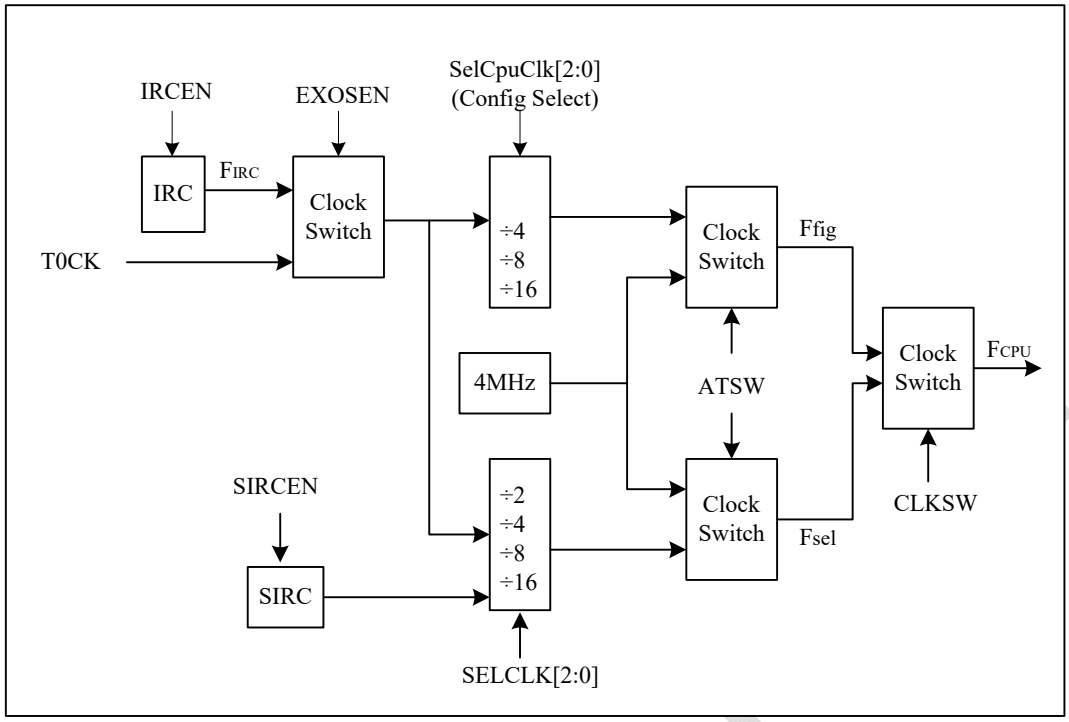


Figure 4.0-1 Clock Switch Block diagram

Example : Clock Switch demo code(MCU clock is 1Mhz when selCpuClk == 3'b001)
Switch MCU clock from Ffig to Fsel (Fcpu=8Mhz)

```
BCR     CLKCFG , SELCLK2_B
BCR     CLKCFG , SELCLK1_B
BSR     CLKCFG , SELCLK0_B
                                //
BCR     CLKCFG , ATSW           //  Clear ATSW=0
BCR     CLKCFG, EXOSEN          //  SET EXOSEN=0
                                //  Fcpu Switch to Ffig
BCR     CLKCFG , SELCLK2_B
BSR     CLKCFG , SELCLK1_B
BSR     CLKCFG , SELCLK0_B      // Select  Fcpu clock = Fsel  (8MHz)

 BSR    CLKCFG , CLKSW          //  Fcpu Switch to Fsel=8Mhz(Now Fcpu = 8Mhz)
```

Example : clock switch demo code(MCU clock is 1Mhz when selCpuClk == 3'b001)
Switch MCU clock from Ffig to Fsel (Fcpu=8Mhz)

```
BCR     CLKCFG , SELCLK2_B
BSR     CLKCFG , SELCLK1_B
BSR     CLKCFG , SELCLK0_B

BCR     CLKCFG , ATSW           // Clear ATSW=0
 BCR    CLKCFG, EXOSEN          //  SET EXOSEN=0
                                //  Fcpu Switch to Ffig
BSR     CLKCFG , SELCLK2_B
BCR     CLKCFG , SELCLK1_B
BSR     CLKCFG , SELCLK0_B      //  Select Fcpu clock = Fsel  (FSIRC)

 BSR    CLKCFG , CLKSW          //  Fcpu Switch to Fsel=SIRC 32KHz(Now Fcpu = 32Khz)
```

【5】 System Operating Mode

5.1 Overview

The FM8PC712 support a versatile low-power operation mode as bellows:

(1) Normal Mode.
(2) Slow Mode.
(3) Green Mode.
(4) Suspend Mode

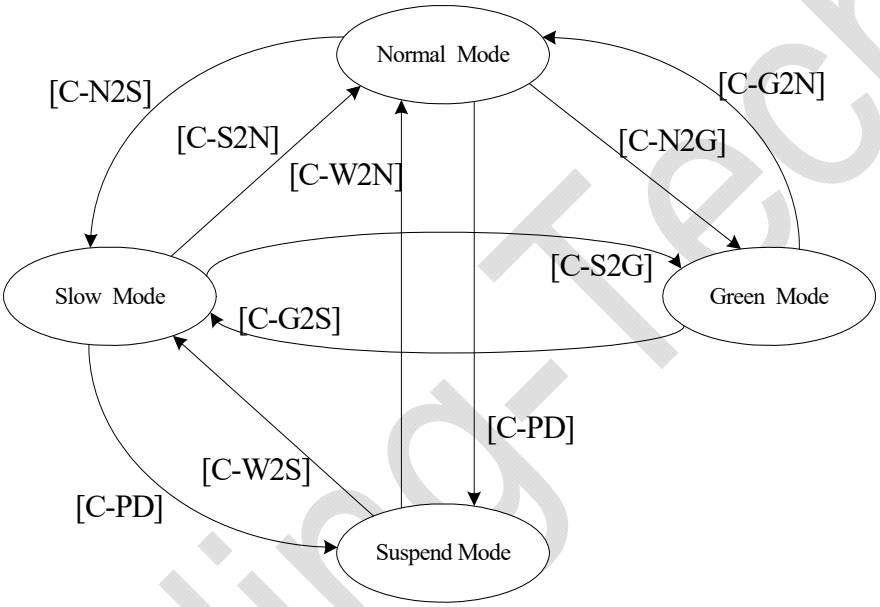


Figure 5.1-1 System Switch Mode Block diagram

Condition Description for System switch mode :

[C-PD] : Normal mode or Slow mode into Power down condition.
Set SUSPEND (Reg.12h.7) bit to 1

Example:

```
Sleep                    // Sleep instruction
NOP
NOP
```

[C-W2N] : Suspend mode wakeup to Normal mode condition.
(1) INT0,INT1 wakeup interrupt.
(2) external Reset occurs.

Note : If system is from Normal mode to suspend mode, the system will be from suspend mode to normal mode when wakeup interrupt occurs.

[C-W2S] : Suspend mode wakeup to Slow mode condition.
(1) IN0,INT1 wakeup interrupt.
(2) LVR or external Reset occurs.

Note : If system is from Slow mode to suspend mode, the system will be from suspend mode to Slow mode when wakeup interrupt occurs.

[C-N2S] : Normal mode into Slow mode condition.
First, the firmware needs to switch CPU clock, the CPU clock will be from FIRC/FOSC to FSIRC.
Next, set LVDIS (Reg.12h.5) bit to 1

Example code:

```
BSR    CLKCFG, SELCLK2_B          // set Fsel = FSIRC (SELCLK=3'b101)
BCR    CLKCFG, SELCLK1_B
BSR    CLKCFG, SELCLK0_B
BSR    CLKCFG, CLKSW_B            // switch CPU clock
NOP

BSR    PCON, LVDIS_B
```

[C-S2N] : Slow mode into normal mode condition.
When the firmware switches CPU clock from FSIRC to FIRC/FOSC and sets LVDIS (Reg.12h.5) bit to 0.

Example code:

```
BCR    PCON, LVDIS_B
BCR    CLKCFG, CLKSW_B            // switch CPU clock
```

[C-N2G] : Normal mode into Green mode condition.
Green mode is sort into two types. Their difference is one disables all LVD36, LVD24, LVD20 and internal high IRC, and another not.

Example code for enabling all low voltage detect and internal high IRC:

```
BSR    PCON,GREEN_MD_B        //set GREEN_MD bit to 1
NOP
NOP
```

Example code for disabling all low voltage detect and internal high IRC :

```
MOVIA   0b01100000            //set GREEN_MD and LVDIS bit to 1 at the same time
MOVAR   PCON
NOP
NOP
```

[C-G2N] : Green mode into normal mode condition.
(1) PA,PB wakeup interrupt.
(2) LVR or external Reset occurs.
(3) WDT time out interrupt.
(4) timers time out interrupt.

[C-S2G] : Slow mode into Green mode condition.
Slow mode only can be changed into the Green mode that disable all low voltage detect, because Slow mode always disable low voltage detect. Set GREEN_MD (Reg.12h.6) bit to 1 and enter Green mode.

Example:

```
BSR    PCON, GRN_MD_B
NOP
NOP
```

[C-G2S] : Green mode into Slow mode condition.
(1) PA,PB wakeup interrupt.
(2) LVR or external Reset occurs.
(3) WDT time out interrupt.
(4) 4 timers time out interrupt.

Note : If system is from Slow mode to Green mode, the system will be from Green mode to Slow mode when wakeup interrupt occurs.

Operating Mode Description

MODE / Module	Normal Mode	Slow Mode	Green Mode	Suspend Mode (Power down Mode)
FIRC	Running (IRCEN = 1)	Disable or enable (by IRCEN)	Disable (IRCEN = 0 or 1)	Disable (IRCEN = 0 or 1)
FSIRC	Running (SIRCEN = 1)	Running (SIRCEN = 1)	Running (SIRCEN = 1)	Disable (SIRCEN = 0)
WDT	Running (WDTE = 1, WDTSL=0)	Running (WDTE = 1, WDTSL=0)	Running (WDTE = 1, WDTSL=1)	Disable (WDTE = 0, WDTSL=0)
Internal Interrupt	All enable	All enable	All enable	All enable
External Interrupt	All enable	All enable	All enable	All enable
Wakeup even	--	--	INT0,INT1,INT2,INT3 interrupt Timer, WDT time output , Reset	INT0,INT1,INT2,INT3 interrupt Reset
Sleep instruction	non	non	non	Run
{Green,LVDIS} (In Reg-12h)	2'b00	2'b01	2'b10,2'b11	2'bxx
PC of MCU	Work	Work	Stop	Stop
Clock of MCU	FOSC or FIRC	FSIRC	Non clock	Non clock

【6】 PWM Description

6.0 PWM/Buzzer Overview

The PWM0 modules is pulse modulator combined with 12-bit generator. The FM8PC712AH supports two channels PWM0(PA[3])/PWM1 output. The PWM output timing is as follow Figure 8-1.

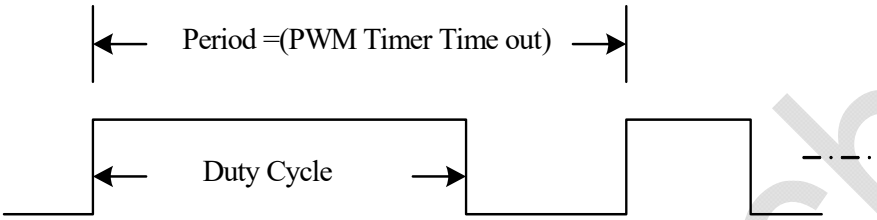


Figure 6-1 PWM Timing

Duty cycle is define by as following:

Duty Cycle = ((TMRLD) == PWM counter);

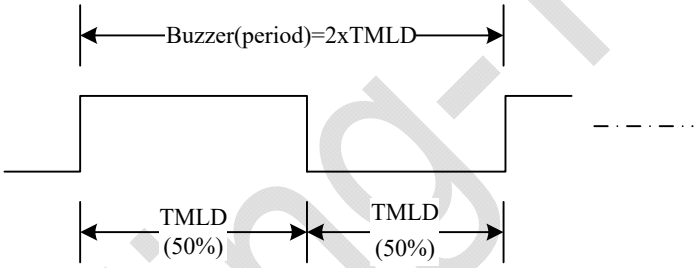


Figure 6-2 Buzzer Timing

Buzzer(Period) = 2 X((TMLD+1)== PWM counter)

Period calibrated :

(A) As **PWM mode** : (PWMXEN=1,PXTMEN=1, **BZX=0**):

Period = (PWM counter == $2^{Timer-bits}$) * (Tp0ck)

Example : P0DT[2:0] = 3'b000 (select 8-bit counter) ,
P0CKS[2:0] = 3'b001 (Fp0ck /2)
P0TPS[2:0] = 3'b001(Fp0ck = FIRC)
Period = 2^8 * 2 * 1/ FIRC = 256 * 2 * 62.5ns = 32 us

(B) As **Timer mode** : (PWMXEN=0,PXTMEN=1, **BZX=0**):

Period = (PWM counter == TMRLD) * (Tp0ck)

Example : Fcpu = 1MHz
P0DT[2:0] = 3'b101 (select 10-bit counter) ,
P0TPS[2:0] = 3'b000 (Fp0ck)
P0CKS[2:0] = 3'b000 (Fp0ck = Fcpu) and TMRLD= 3E8 h

Timer Time out = 3E8 * 1/ Fp0ck = 1000 * 1/ Fcpu = 1000 * 1us = 1ms

(C) As Buzzer mode : (PWMXEN=0,PXTMEN=1,**BZX=1**)

Period = 2*(PWM counter == (TMRLD+1)) * (Tp0ck)

Example : Fcpu = 1MHz
P0DT[2:0] = 3'b101 (select 10-bit counter) ,
P0TPS[2:0] = 3'b000 (Fp0ck)
P0CKS[2:0] = 3'b000 (Fp0ck = Fcpu) and TMRLD= 3E7 h

Buzzer period = 2* (3E7+1) * 1/ Fp0ck = 2* 1000 * 1/ Fcpu = 2000 * 1us = 2ms (0.5KHz)

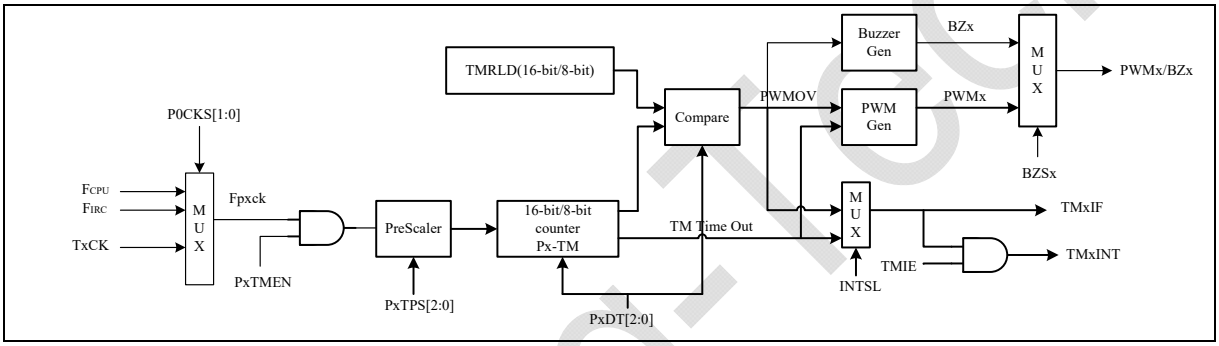


Figure 6-3 PWM0/Buzzer0/PWM1/Buzzer1 Block diagram

6.1 PWM0 Register

Address 14H: PWM0 configuration Register(PWM0CON)

Bits	7	6	5	4	3:2	1~0
Name	P0INTSL	P0DT[2:0]			P0CKS[1:0]	P0OSEL[1:0]
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	2'b00	2'b00

Bit[7] : P0INTSL

PWM0 interrupt selection.
1 = Select interrupt for PWM0 overflow.
0 = Select interrupt for PWM0 timer time out.

Bit[6:4] :P0DT[2:0]

PWM0 Duty Range.

P0DT[[2:0],	PWM0 Duty Range		PWM0 Timer bits
	High pulse	Low Pulse	
3'b000	1~256	256~1	8 bits
3'b001	1~512	512~1	9 bits
3'b010	1~1024	1024~1	10 bits
3'b011	1~2048	2048~1	11 bits
3'b100	1~4096	4096~1	12 bits
3'b101	1~16384	16384~1	14 bits
3'b110	1~32768	32768~1	15 bits
3'b111	1~65536	65536~1	16 bits

TABLE 6-3 PWM0 Duty Range

Bit[3:2] : P0CKS[1:0]

PWM0 Timer clock select.

P0CKS[2:0]	Clock select (Fp0ck)
2'b00	Fcpu
2'b01	FIRC (16Mhz)
2'b10	--
2'b11	T0CK(External clock)

Bit[1:0] : P0OSEL[1:0]

PWM0/Buzzer0 output select

P0OSE [2:0]	Output PIN
2'b00	PA[3]
2'b01	PA[0]
2'b10	PA[1]
--	--

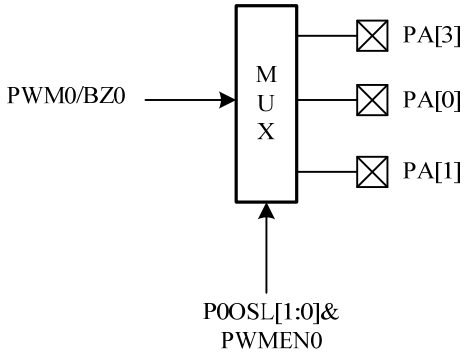


Figure 6-4 PWM0/BZ0 pin select

Address 15H: PWM0 Control Register (PWM0CR)

Bits	7	6	5	4	3	2	1	0
Name	PWM0EN	P0OUTS	P0TPS[2:0]			P0TMEN	P0TMIE	P0TMIF
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7] : PWM0EN
PWM0 module enable.
1 = PWM mode.
0 = Timer mode.

Bit[6] : P0OUTS
PWM0 Duty Cycle pulse output select.
1 = PWM0 Duty Cycle pulse output is low.
0 = PWM0 Duty Cycle pulse output is high.

Bit[5:3] : P0TPS[2:0]

PWM0 Timer prescaler, as follow Table 8-4:

P0CKSL [2:0]	PWM0 MODE (Tp0ck)
3'b000	PWM0 Timer clock select is Fp0ck
3'b001	PWM0 Timer clock select is Fp0ck /2
3'b010	PWM0 Timer clock select is Fp0ck /4
3'b011	PWM0 Timer clock select is Fp0ck /8
3'b100	PWM0 Timer clock select is Fp0ck /16
3'b101	PWM0 Timer clock select is Fp0ck /32
3'b110	PWM0 Timer clock select is Fp0ck /64
3'b111	PWM0 Timer clock select is Fp0ck /128

Table 8-4 PWM0 Timer clock select

Bit[2] : P0TMEN
PWM0 Timer enable bit.
1 = Enable.
0 = Disable.

Bit[1] : P0TMIE
PWM0 Timer overflow interrupt bit.
1 = Enable interrupt.
0 = Disable interrupt.

Bit[0] : P0TMIF
PWM0 Timer overflow flag bit.
1 = PWM0 Timer overflow has occurred, write 0 clear flag.
0 = PWM0 Timer overflow has not occurred yet.

Address 16H: PWM0 Timer Low byte value Register (P0TMLB)

Bits	7	6	5	4	3	2	1	0
Name	P0TM[7:0]							
Read/Write	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bit[7:0] : P0TM[7:0]
PWM0 Timer Low byte

Address 17H: PWM0 Timer compared or overflow reload Low byte value Register (P0TMRLDLB)

Bits	7	6	5	4	3	2	1	0
Name	P0TMRLD[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7:0] : P0TMRLD[7:0]
PWM0 Timer compared or overflow reload Low byte

Address 18H: PWM0 Timer High byte value Register (P0TMHB)

Bits	7	6	5	4	3	2	1	0
Name	P0TM [15:8]							
Read/Write	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bit[7:4] : P0TM[11:8]
PWM0 Timer High byte.

Address 19H: PWM0 Timer compared or overflow reload Low byte value Register (P0TMRLDHB)

Bits	7	6	5	4	3	2	1	0
Name	P0TMRLD [15:8]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7:0] : P0TMRLD[15:8]
PWM0 Timer compared or overflow reload High byt

6.2 PWM1 Register

Address 20H: PWM1 configuration Register(PWM1CON)

Bits	7	6	5	4	3	2	1	0
Name	P1INTSL	P1DT[2:0]			P1CKS[1:0]		P1OSEL[1:0]	
Read/Write	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7] : P1INTSL

PWM1 interrupt selection.
1 = Select interrupt for PWM1 overflow.
0 = Select interrupt for PWM1 timer time out.

Bit[6:4] :P1DT[2:0]

PWM1 Duty Range.

P1DT[[1:0],	PWM1 Duty Range		PWM1 Timer bits
	High pulse	Low Pulse	
3'b000	1~256	256~1	8 bits
3'b001	1~128	128~1	7 bits
3'b010	1~64	64~1	6 bits
3'b011	1~32	32~1	5 bits
3'b100	--	--	--
3'b101	--	--	--
3'b110	--	--	--
3'b111	--	--	--

TABLE 6-3 PWM1 Duty Range

Bit[3:2] : P1CKS[1:0]

PWM1 Timer clock select.

P1CKS[2:0]	Clock select (Fp1ck)
2'b00	Fcpu
2'b01	FIRC (16Mhz)
2'b10	--
2'b11	T0CK(External clock)

Bit[1:0] : P1OSEL[1:0]

PWM1/Buzzer1 output select

P1OSE [2:0]	Output PIN
2'b00	PB[3]
2'b01	PB[0]
2'b10	PB[1]
2'b11	PB[2]

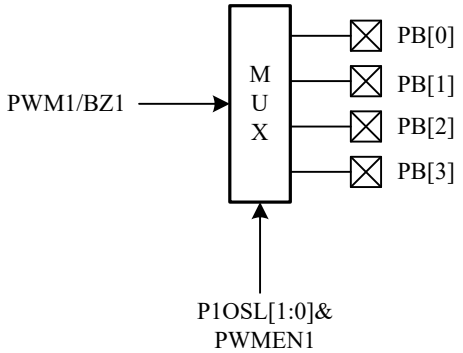


Figure 6-4 PWM1/BZ1 pin select

Address 21H: PWM1 Control Register (PWM1CR)

Bits	7	6	5	4	3	2	1	0
Name	PWM1EN	P1OUTS	P1TPS[2:0]			P1TMEN	P1TMIE	P1TMIF
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7] : PWM1EN
PWM1 module enable.
1 = PWM mode.
0 = Timer mode.

Bit[6] : P1OUTS
PWM1 Duty Cycle pulse output select.
1 = PWM1 Duty Cycle pulse output is low.
0 = PWM1 Duty Cycle pulse output is high.

Bit[5:3] : P1TPS[2:0]
PWM1 Timer prescaler, as follow Table 8-4:

P1CKSL [2:0]	PWM1 MODE (Tp1ck)
3'b000	PWM1 Timer clock select is Fp1ck
3'b001	PWM1 Timer clock select is Fp1ck /2
3'b010	PWM1 Timer clock select is Fp1ck /4
3'b011	PWM1 Timer clock select is Fp1ck /8
3'b100	PWM1 Timer clock select is Fp1ck /16
3'b101	PWM1 Timer clock select is Fp1ck /32
3'b110	PWM1 Timer clock select is Fp1ck /64
3'b111	PWM1 Timer clock select is Fp1ck /128

Table 8-4 PWM0 Timer clock select

Bit[2] : P1TMEN
PWM1 Timer enable bit.
1 = Enable.
0 = Disable.

Bit[1] : P1TMIE
PWM1 Timer overflow interrupt bit.
1 = Enable interrupt.
0 = Disable interrupt.

Bit[0] : P1TMIF
PWM1 Timer overflow flag bit.
1 = PWM1 Timer overflow has occurred, write 0 clear flag.
0 = PWM1 Timer overflow has not occurred yet.

Address 22H: PWM1 Timer Low byte value Register (P1TMLB)

Bits	7	6	5	4	3	2	1	0
Name	P1TM[7:0]							
Read/Write	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bit[7:0] : P1TM[7:0]
PWM1 Timer Low byte

Address 23H: PWM1 Timer compared or overflow reload Low byte value Register (P1TMRLD)

Bits	7	6	5	4	3	2	1	0
Name	P1TMRLD[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7:0] : P1TMRLD[7:0]
PWM1 Timer compared or overflow reload byte

6.3 Buzzer Register

Address 24H:Buzzer output Select Register(BZS)

Bits	7	6	5~0
Name	BZS1	BZS0	Revered
Read/Write	R/W	R	R/W
Default	0	0	6'h00

Bit[7] : BZS1
Buzzer1 output select
1: Enable buzzer1 output to PWM1 PIN (when PWMEN1=1).
0: Disable buzzer1 output .

Bit[6] : BZS0
Buzzer0 output select
1: Enable buzzer0 output to PWM2 PIN (When PWMEN0=1).
0: Disable buzzer0 output .

6.4 PWM Code Example

```
// pwm Clock  F0ck = Fcpu(4MHz)
        BCR     PWM0CON,P0CKS2_B
        BCR     PWM0CON,P0CKS1_B
        BCR     PWM0CON,P0CKS0_B
 // pwm Clock F0ck/32 Hz
        BSR     PWM0CR,P0TPS2_B             // F0ck = 4/32 Mhz = 125 Khz ;
        BCR     PWM0CR,P0TPS1_B
        BSR     PWM0CR,P0TPS0_B
```

(A) 8 bits PWM

```
 // pwm Period Range  8bits(Range 0~255)
        BCR     PWM0CON,P0DT2_B
        BCR     PWM0CON,P0DT1_B
        BCR     PWM0CON,P0DT0_B

        MOVIA   00fh                    // Set P0TMRLD[7:0] value
        MOVAR   P0TMRLDLB               // Duty Width = 15 (1/F0ck) clock

// pwm Enable
        BSR     PWM0CR,P0TMIE_B
        BSR     PWM0CR, PWM0EN_B            // Set PWM0EN_B
        BSR     PWM0CR, P0TMEN_B
```

(B)16 bits PWM

```
 // pwm  Period Range 12bits( Rang 0~65536)
        BSR     PWM0CON,P0DT2_B
        BSR     PWM0CON,P0DT1_B
        BSR     PWM0CON,P0DT0_B

        MOVIA   0x00h                   // Load P0TMRLD[7:0] value
        MOVAR   P0RDLB                  //
        MOVIA   0x80h                   // Load P0TMRLD[15:8] value
        MOVAR   P0RDHB                  // Duty Width = 32768 (1/F0ck) clock

  // pwm Enable
        BSR     PWM0CR,P0TMIE_B
        BSR     PWM0CR, PWM0EN_B            // Set PWM0EN_B
        BSR     PWM0CR, P0TMEN_B
```

(C)8 bits PWM Switch to 16 bits PWM

```
// pwm Periode =8bit (Range 1~256)
        BCR     PWM0CON,P0DT2_B
        BCR     PWM0CON,P0DT1_B
        BCR     PWM0CON,P0DT0_B

      MOVIA   00fh                  //  Set  P0TMRLD[7:0] value
      MOVAR  P0TMRLDLB

  // pwm enable
        BSR     PWM0CR,P0TMIE_B
        BSR     PWM0CR, PWM0EN_B          //  Set PWM0EN_B
        BSR     PWM0CR, P0TMEN_B

// pwm Period 16bits (Range 1~65536)
        MOVIA   00fh                  //  Set  P0TMRLD[7:0] value
        MOVAR  P0TMRLDLB
        MOVIA   00h                   //  Set  P0TMRLD[15:8] value
        MOVAR  P0TMRLDHB

        MOVIA   8Fh
        ANDAR   PWM0CON,R             //  Clear P0DT2[2:0]
         MOVIA   30h
         IORAR    PWM0CON,R           // Switch to 16 bits
```

(D) 12bits PWM reload updated

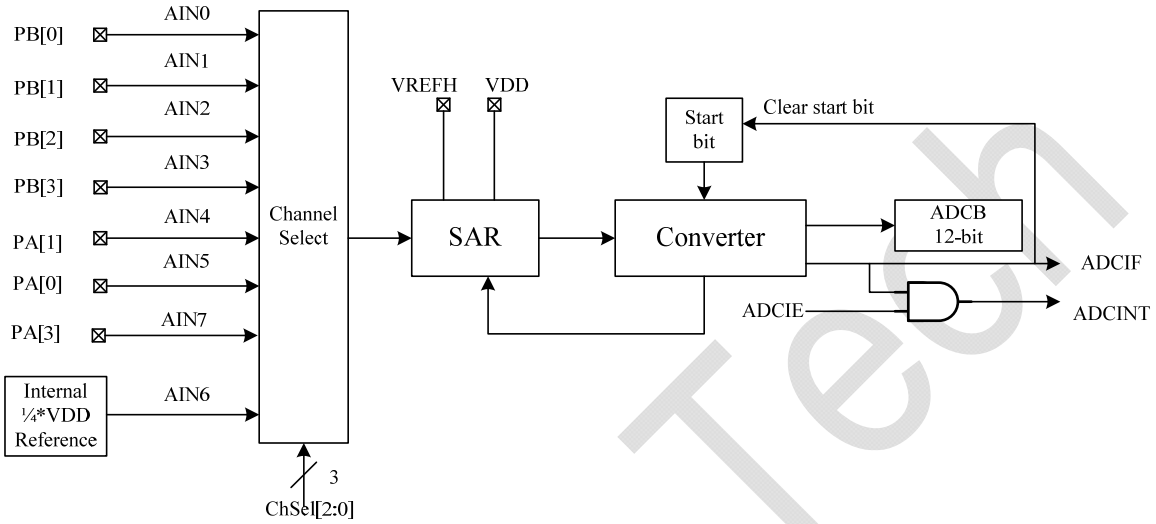
```
// pwm  Period Range=12bits  (Range 1~4096)
        BSR     PWM0CON,P0DT2_B
        BCR     PWM0CON,P0DT1_B
        BCR     PWM0CON,P0DT0_B
      // Reload value
       MOVIA   007h                  //  Set  P0TMRLD[7:0] value
        MOVAR  P0RDLB                //
        MOVIA   10h                   //  Set  P0TMRLD[15:8] value
        MOVAR  P0RDHB

  // pwm Enable
        BSR     PWM0CR,P0TMIE_B
        BSR     PWM0CR, PWM0EN_B          // Set PWM0EN_B
        BSR     PWM0CR, P0TMEN_B

 // Reload updated
        MOVIA   02Ch                  //  Set  P0TMRLD[7:0] value
        MOVAR  P0RDLB                 //
        MOVIA   10h                   //  Set  P0TMRLD[15:8] value
        MOVAR  P0RDHB                 //  Duty Width from 1007h switch to  102Ch
```

【7】 7+1 Channel Analog to Digital (ADC)

Build In ADC module supports 7 channel(PB[0]~PB[3],PA[0],PA[1],PA[3]) and one internal channel ¼ VDD reference that can be use for auxiliary input and battery monitor. The ADC module converts an input voltage to a 12-bit digital code.



7.1 ADC Registers

Address 28H: ADC Control _1 Register(ADCON_1)

Bits	7	6	5	4	3	2	1	0
Name	ADCEN	ADCST	CHSEL[2:0]			--	ADCSR[1:0]	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7] : ADCEN

ADC module enable bit.
1 = Enable ADC.
0 = Disable ADC.

Bit[6] : ADCST

1 = Start to ADC sample, when ADC conversion has been completed, this start be clear to 0 by H/W.
0 = Stop.

Bit[5:2] : CHSEL[2:0]

ADC input channel select bit, as follows Table9-1

CHSEL[2:0]	Input Channel
3'b000	PB[0] (AIN0)
3'b001	PB[1] (AIN1)
3'b010	PB[2] (AIN2)
3'b011	PB[3] (AIN3)
3'b100	PA[1] (AIN4)
3'b101	PA[0] (AIN5)
3'b110	Internal VDD/4 (AIN6)
3'b111	PA[3] (AIN7)

Table 9-1 ADC input channel select

Bit[1:0] : ADCSR[1:0]

ADC clock selection.
2'b00 : ADC clock is Fcpu/8 .
2'b01 : ADC clock is Fcpu/4 .
2'b10 : ADC clock is Fcpu/2 .
2'b11 : ADC clock is Fcpu .

Address 29H: ADC Control_2 Register(ADCON_2)

Bits	7	6	5	4	3	2	1	0
Name	ADCIE	ADCIF	SVREFH	ADCNT	SELH	ADCTMS	SELVER[1:0]	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7] : ADCIE

ADC interrupt Enable bit .
1 = Enable.
0 = Disable.

Bit[6] : ADCIF

ADC conversion has been completed interrupt flag.
1 = ADC conversion has been completed, write 0 clear flag.
0 = ADC conversion has been not completed yet.

Bit[5] : SVREFH

Select VREFH from external or internal voltage.
1 = External voltage(VREFH == PB[1] or PB[3] pin) base on bit[3].
0 = Internal voltage(VREFH == Internal reference voltage Table9-2).

Bit[4] : ADCNT

ADC sample mode.
1 = ADC continues mode.
0 = Trigger mode base on ADCST bit.

Bit[3] : SELH

External VREFH selection
1 = select external VREFH form PB[1]
0 = select external VREFH form PB[3]

Bit[3] : ADCTMS

ADC convert Timing.
1 = Fixed convert timing.
0 = Non-Fixed convert timing.

Bit[1:0] : SELVER[1:0]

ADC internal VERFH voltage selection.

SELVER[1:0]	VREFH
2'b00	VDD
2'b01	4V
2'b10	3V
2'b11	2V

Table 9-2 ADC internal VERFH voltage selection

Address 30H: ADC High byte Register(ADCHB)

Bits	7	6	5	4	3	2	1	0
Name	ADCB[11:4]							
Read/Write	R							
Default	0	0	0	0	0	0	0	0

Bit[7:0] : ADCB[11:4] read only when ADCEN=1
ADC High data byte of ADCB[11:0] buffer

Address 31H: ADC Low byte Register(ADCLB)

Bits	7~4	3~0
Name	Revered	ADCB[3:0]
Read/Write	--	R
Default	0	0

Bit[3:0] : ADCB[3:0] read only
ADC Low data byte of ADCB[11:0] buffer.

Address 32H: ADC Control_3 Register(ADCON_3)

Bits	7	6	5	4	3	2	1	0
Name	AIN[7]	Revered	INEN[5]	INEN[4]	INEN[3]	INEN[2]	INEN[1:0]	
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7] : Revered
PA[3] input circuit enable (AIN7).
1 = Disable . (As Sleep mode the AIN7 is analog signal)
0 = Enable.

Bit[6] : Revered

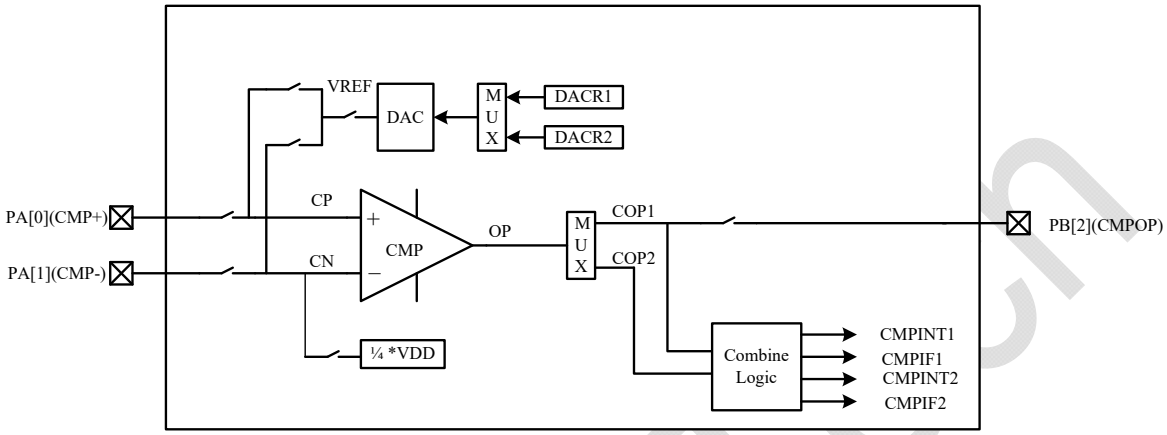
Bit[5] : INEN[5]
PA[0] input circuit enable (AIN5).
1 = Disable . (As Sleep mode the AIN5 is analog signal)
0 = Enable.

Bit[4] : INEN[4]
PA[1] input circuit enable (AIN4)
1 = Disable . (As Sleep mode the AIN4 is analog signal)
0 = Enable.

Bit[3:0] : INEN[3:0]
PB[3:0] input circuit enable (AIN3/AIN2/AIN1/AIN0).
1 = Disable . (As Sleep mode the AIN3/AIN4/AIN1/AIN0 is analog signal)
0 = Enable.

【8】 Voltage Comparator

The FM8PC712AH build in one low input offset voltage comparator.
The comparator input/output are sharing with GPIO pin and the block diagram as follow:



8.1 CMP Registers

Address 35H : Comparator control Register-1(CMPCON1)

Bits	7	6	5	4	3	2	1	0
Name	CMPEN	COP1	CMPIE1	CMPRIF1	CMPFIF1	CMPMD[2:0]		
Read/Write	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7] : CMPEN
Comparator enable/Disable.
1 = Enable.
0 = Disable.

Bit[6] : COP1
Comparator output signal of DACR1.
1 = CP > CN
0 = CP < CN

Bit[5] : CMPIE1
Comparator Interrupt enable bit.
1 = Enable Comparator Interrupt of DACR1.
0 = Disable Comparator Interrupt of DACR1

Bit[4] : CMPRIF1
CMPPIF is interrupt flag of DACR1, write 0 clear flag.
1 = Interrupt occurrence when Comparator output of DACR1 is raising (CP>CN).

Bit[3] : CMPFIF1
CMPFIF is interrupt flag of DACR1, write 0 clear flag.
1 = Interrupt occurrence when Comparator output of DACR1 is falling (CP<CN).

Bit[2:0]: CMPMD[2:0]

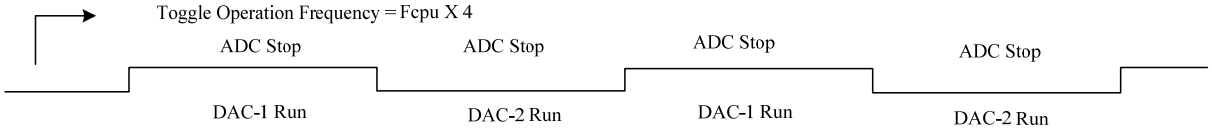
Comparator operation mode as **Table 8-1**

CMPEN	CMPMD[2:0]	Description			
		PA[0]	PA[1]	PB[2]	Functional Description
0	3'bXXX	GPIO	GPIO	GPIO	Disable Comparator
1	3'b111	CP	CN	COP	Enable comparator PA[0] → CP PA[1] → CN COP → PB[2]
1	3'b101	CP	GPIO	COP	Enable comparator PA[0] → CP PA[1] is GPIO CN → DAC(VREF) COP1 → PB[2] (The operation mode is as Table 8-2)
1	3'b011	GPIO	CN	COP	Enable comparator PA[0] is GPIO CP → DAC(VREF) PA[1] → CN COP1 → PB[2] (The operation mode is as Table 8-2)
1	3'b110	CP	CN	GPIO	Enable comparator PA[0] → CP PA[1] → CN PB[2] is GPIO (COP1 output)
1	3'b100	CP	GPIO	GPIO	Enable comparator PA[0] → CP PA[1] is GPIO CN → DAC(VREF) PB[2] is GPIO (The operation mode is as Table 8-2)
1	3'b010	GPIO	CN	GPIO	Enable comparator PA[0]is GPIO CP → DAC(VREF) PA[1] → 1/4 VDD PB[2] is GPIO (The operation mode is as Table 8-2)

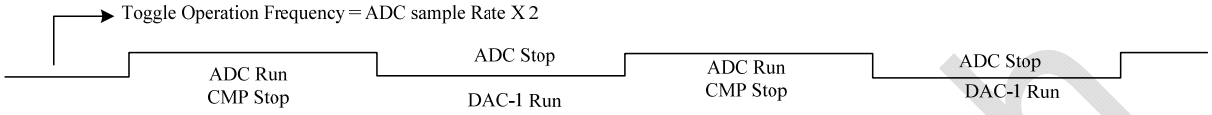
The operation Mode **Table 8-2**

ADCEN	TOGSEL	Functional Description
0	0	The DAC-1(DACR1) of CMP is real operation mode **TMD-0**
0	1	The DAC-1(DACR1) and DAC-2(DACR2) CMP is toggle operation mode **TMD-1**
1	0	The ADC and DAC-1(DACR1) of CMP is toggle operation mode **TMD-2**
1	1	The ADC and CMP DAC-1(DACR1) and DAC-2(DACR2) is toggle operation mode **TMD-3**

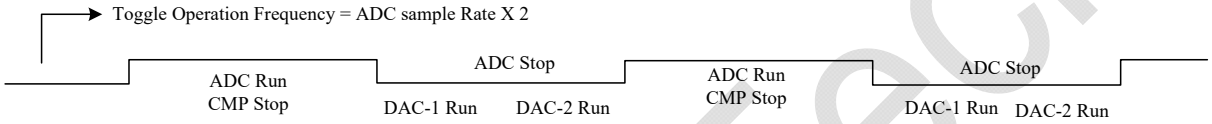
TMD-1 operation Timing :



TMD-2 operation Timing :



TMD-3 operation Timing :



Address 36H:DAC High byte Register-1(DACR1HB)

Bits	7	6	5	4	3	2	1	0
Name	DACR1[11:4]							
Read/Write	R/W	R /W	R/W	R /W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7:0] : DACR1[11:4]

DACR1 High byte data .

Address 37H: DAC Low byte Register-1(DACR1LB)

Bits	7~4	3~0
Name	Revered	DACR1[3:0]
Read/Write	--	R/W
Default	0	0

Bit[3:0] : DACR1[3:0]

DACR1 Low byte Data

Address 38H : Comparator control Register-2(CMPCON2)

Bits	7	6	5	4	3	2	1	0
Name	CMPINT1	COP2	CMPIE2	CMPRIF2	CMPFIF2	CMPINT2	TOGSEL	Revered
Read/Write	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7] : CMPINT1
1 = CMPINT1 Pin-Change to interrupt.
0 = CMPINT1 falling edge to interrupt.

Bit[6] : COP2
Comparator output signal of DACR2.
1 = CP > CN
0 = CP < CN

Bit[5] : CMPIE2
Comparator Interrupt of DACR2 enable bit.
1 = Enable Comparator Interrupt of DACR2.
0 = Disable Comparator Interrupt of DACR2

Bit[4] : CMPRIF2
CMPPIF2 is interrupt of DACR2 flag, write 0 clear flag.
1 = Interrupt occurrence when Comparator output of DACR2 is raising (CP>CN).

Bit[3] : CMPFIF2
CMPFIF2 is interrupt flag of DACR2, write 0 clear flag.
1 = Interrupt occurrence when Comparator output of DACR2 is falling (CP<CN).

Bit[2] : CMPINT2
1 = CMPINT2 Pin-Change to interrupt.
0 = CMPINT2 falling edge to interrupt.

Bit[1] : TOGSEL
ADC and CMP toggle operation selection.**(As Table 8-2)**

Address 39H:DAC High byte Register-2(DACR2HB)

Bits	7	6	5	4	3	2	1	0
Name	DACR2[11:4]							
Read/Write	R/W	R /W	R/W	R /W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7:0] : DACR2[11:4]

DACR2 High byte data .

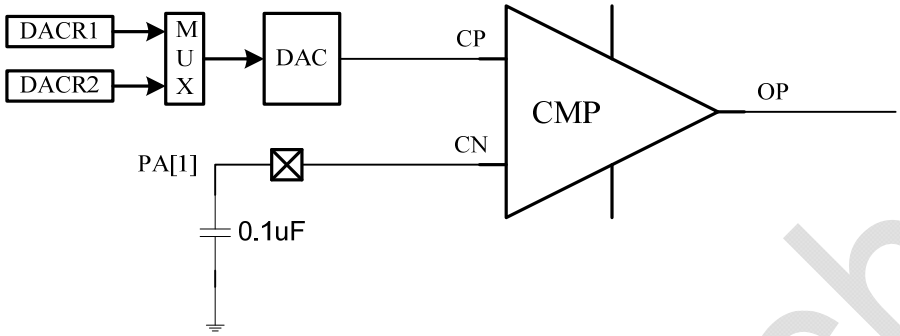
Address 3AH: DAC Low byte Register-2(DACR2LB)

Bits	7~4	3~0
Name	Revered	DACR2[3:0]
Read/Write	--	R/W
Default	0	0

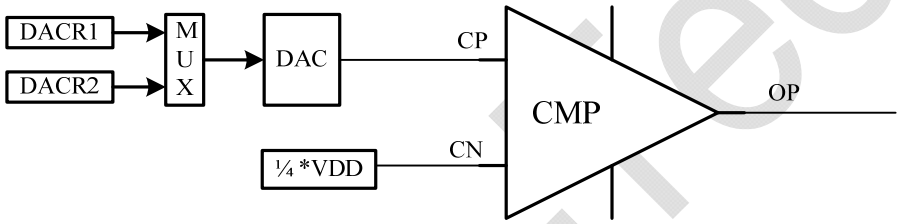
Bit[3:0] : DACR2[3:0]

DACR2 Low byte Data

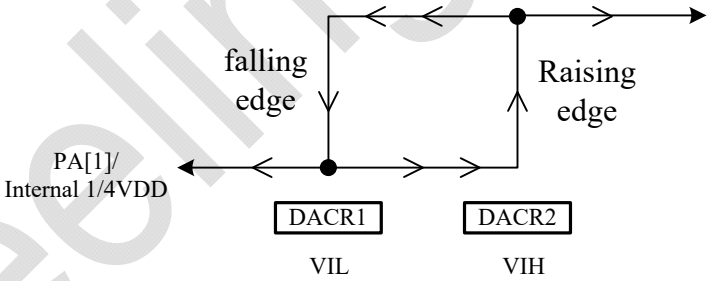
8.2 Comparator with Hysteresis Application



8.2-1 Compared External PA[1] Hysteresis application(TMD-1/TMD-3)



8.2-2 Compared Internal 1/4 VDD Hysteresis application(TMD-1/TMD-3)

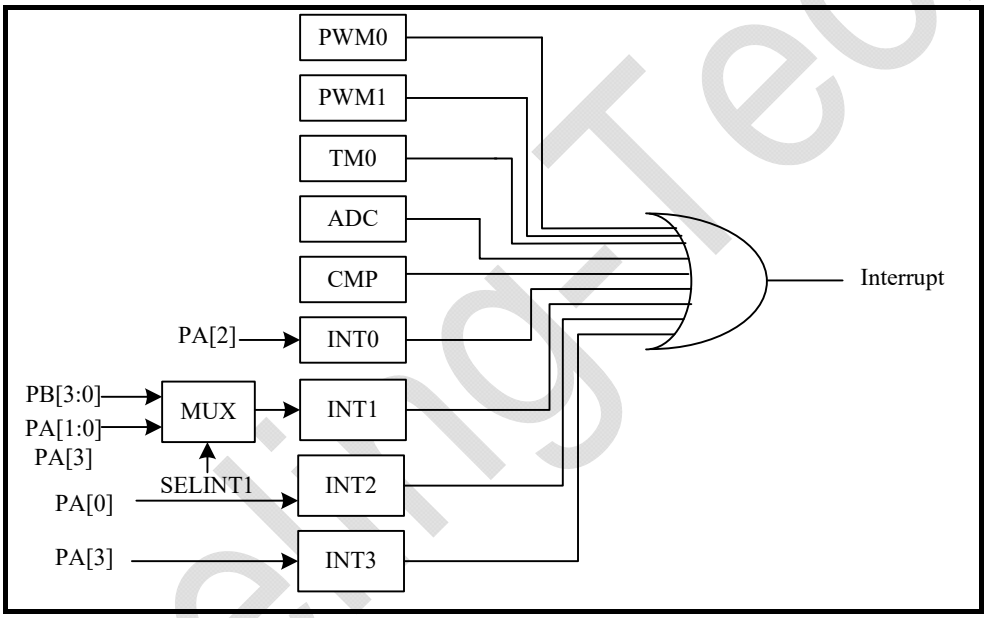


8.2-3 Hysteresis Diagram of PA[1] or 1/4VDD

【9】 Interrupt

The FM8PC712AH has interrupt as following:
(1) PWM0 /PWM1 interrupt.
(2) TM0 Timer interrupt.
(3) INT0, INT1 ,INT2, INT3 external interrupt.
(4) ADC sample completed interrupt.
(5) Comparator output has changed interrupt.

The FM8PC712AH reset vector is fixed at **0x0000h** and
the interrupt vector is at **0x0003h.**
A global interrupt enable bit, GIE(Reg.0Bh-7), enable(if set) all un-masked interrupts or disables(if cleared) all interrupts. Individual interrupts can be enable/disable through their corresponding enable bits in INTEN register regardless of the status of the GIE bit.
The interrupt priority is decided by customer firmware control.



Interrupt Block Diagram

9.1 Interrupt Registers

Address 0BH : Interrupt Mask Register(INTEN)

Bits	7	6	5	4	3	2	1	0
Name	GIE	Revered	Revered	INT3IE	INT2IE	INT1IE	INT0IE	TM0IE
Read/Write	R/W	R	R	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7] : GIE
Global Interrupt enable bit.
1 = Enable.
0 = Disable.

Bit[6:5] : Revered

Bit[4] : INT3IE
INT1IE Interrupt enable bit.
1 = Enable.
0 = Disable.

Bit[3] : INT2IE
INT1IE Interrupt enable bit.
1 = Enable.
0 = Disable

Bit[2] : INT1IE
INT1IE Interrupt enable bit.
1 = Enable.
0 = Disable.

Bit[1] : INT0IE
Global Interrupt enable bit.
1 = Enable.
0 = Disable.

Bit[0] : TM0IE
Timer 0 Interrupt enable bit.
1 = Enable.
0 = Disable.

Address 0CH : Interrupt Flag Register(INTFLAG)

Bits	7	6	5	4	3	2	1	0
Name	--	--	--	INT3IF	INT2IF	INT1IF	INT0IF	TM0IF
Read/Write	R	R	R	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[4] :INT3IF
INT3 interrupt flag, write 0 clear flag.
1 = Interrupt occurrence of INT3(PA[3]).

Bit[3] :INT2IF
INT2 interrupt flag, write 0 clear flag.
1 = Interrupt occurrence of INT2(PA[0]).

Bit[2] :INT1IF
INT1 interrupt flag, write 0 clear flag.
1 = Interrupt occurrence of INT1(PA[1]).

Bit[1] :INT0IF
INT0 interrupt flag(INT0 falling edge), write 0 clear flag.
1 = Interrupt occurrence of INT0[PA[2]].

Bit[0] :TM0IF
Timer0 interrupt flag, write 0 clear flag.
1= Timer 0 Timer out and interrupt occurrence.

Address 0DH : Interrupt Control Register(INTCON)

Bits	7	6	5	4	3	2	1	0
Name	SELINT1[2]	SELINT1[1]	SELINT1[0]	INT3CON	INT2CON	INT1CON	INT0CON	--
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	-R
Default	0	0	0	0	0	0	0	0

Bit[7:5] : SELINT1[1:0]
Select INT1 Which pin is interrup1

SELINT[2:0]	Select GPIO
3'b000	PA[1]
3'b001	PA[0]
3'b010	PA[3]
3'b011	PB[0]
3'b100	PB[1]
3'b101	PB[2]
3'b110	PB[3]

Bit[3] :INT3CON

1 = INT3 Pin-Change to interrupt.
0 = INT3 falling edge to interrupt.

Bit[2] :INT2CON

1 = INT2 Pin-Change to interrupt.
0 = INT2 falling edge to interrupt.

Bit[2] :INT1CON

1 = INT1 Pin-Change to interrupt.
0 = INT1 falling edge to interrupt.

Bit[1] :INT0CON

1 = INT0 Pin-Change to interrupt.
0 = INT0 falling edge to interrupt.

【10】 Instruction Set

Mnemonic, Operands		Description	Operation	Cycles	Status Affected
BCR	R, bit	Clear bit in R	0 → R<b>	1	-
BSR	R, bit	Set bit in R	1 → R<b>	1	-
BTRSC	R, bit	Test bit in R, Skip if Clear	Skip if R<b> = 0	1/2 (1)	-
BTRSS	R, bit	Test bit in R, Skip if Set	Skip if R<b> = 1	1/2 (1)	-
NOP		No Operation	No operation	1	-
CLRWDT		Clear Watchdog Timer	00h → WDT, 00h → WDT prescaler	1	$\overline{TO}$, $\overline{PD}$
SLEEP		Go into power-down mode	00h → WDT, 00h → WDT prescaler	1	$\overline{TO}$, $\overline{PD}$
RETURN		Return from subroutine	Top of Stack → PC	2	-
RETFIE		Return from interrupt, set GIE bit	Top of Stack → PC, 1 → GIE	2	-
CLRA		Clear ACC	00h → ACC	1	Z
IOST	R	Load R-plane register	ACC → R-plane register	1	-
IOSTR	R	Read R-plane register	R-plane register → ACC		
CLRR	R	Clear R	00h → R	1	Z
MOVAR	R	Move ACC to R	ACC → R	1	-
MOVR	R, d	Move R	R → dest	1	Z
DECR	R, d	Decrement R	R - 1 → dest	1	Z
DECRSZ	R, d	Decrement R, Skip if 0	R - 1 → dest, Skip if result = 0	1/2 (1)	-
INCR	R, d	Increment R	R + 1 → dest	1	Z
INCRSZ	R, d	Increment R, Skip if 0	R + 1 → dest, Skip if result = 0	1/2 (1)	-
ADDAR	R, d	Add ACC and R	R + ACC → dest	1	C, DC, Z
SUBAR	R, d	Subtract ACC from R	R - ACC → dest	1	C, DC, Z
ADCAR	R, d	Add ACC and R with carry	R + ACC + C → dest	1	C, DC, Z
SBCAR	R, d	Subtract ACC from R with Carry	R + $\overline{ACC}$ + C → dest	1	C, DC, Z
ANDAR	R, d	AND ACC with R	ACC and R → dest	1	Z
IORAR	R, d	Inclusive OR ACC with R	ACC or R → dest	1	Z
XORAR	R, d	Exclusive OR ACC with R	R xor ACC → dest	1	Z
COMR	R, d	Complement R	$\overline{R}$ → dest	1	Z
RLR	R, d	Rotate left f through Carry	R<7> → C, R<6:0> → dest<7:1>, C → dest<0>	1	C
RRR	R, d	Rotate right f through Carry	C → dest<7>, R<7:1> → dest<6:0>, R<0> → C	1	C
SWAPR	R, d	Swap R	R<3:0> → dest<7:4>, R<7:4> → dest<3:0>	1	-
MOVIA	I	Move Immediate to ACC	I → ACC	1	-
ADDIA	I	Add ACC and Immediate	I + ACC → ACC	1	C, DC, Z
SUBIA	I	Subtract ACC from Immediate	I - ACC → ACC	1	C, DC, Z
ANDIA	I	AND Immediate with ACC	ACC and I → ACC	1	Z

Mnemonic, Operands	Description	Operation	Cycles	Status Affected
IORIA I	OR Immediate with ACC	ACC or I → ACC	1	Z
XORIA I	Exclusive OR Immediate to ACC	ACC xor I → ACC	1	Z
RETIA I	Return, place Immediate in ACC	I → ACC, Top of Stack → PC	2	-
CALL I	Call subroutine	PC + 1 → Top of Stack, I → PC	2	-
GOTO I	Unconditional branch	I → PC	2	-

Note : 1. 2 cycles for skip, else 1 cycle(one Fcpu clock)

2. bit : Bit address within an 8-bit register R
R : Register address (00h to 7Fh)
I : Immediate data
ACC : Accumulator
D : Destination select;
=0 (store result in ACC)
=1 (store result in file register R)
Dest : Destination
PC : Program Counter
PCHBUF : High Byte Buffer of Program Counter
WDT : Watchdog Timer Counter
GIE : Global interrupt enable bit
$\overline{TO}$: Time-out bit
$\overline{PD}$: Power-down bit
C : Carry bit
DC : Digital carry bit
Z : Zero bit

【11】 Absolute Maximum Ratings

10. Absolute Maximum Ratings

Parameter	Conditions	Values		Unit
		min.	max.	
Ambient Operating Temperature	-	-40	85	℃
Storage Temperature	-	-40	150	℃
DC Supply Voltage(VDD)	Respect to VSS	2.4	5.5	V
Supply Current	-	-	-	mA
Voltage on all pin	Respect to VSS	-0.3	VDD+0.3V	V

【12】 DC Characteristics

12.1 General (Operating Temperature = 0 to 70 ℃)

Symbol	Parameter	Conditions	Values			Unit
			MIN.	TYP	MAX	
VDD	Operating Voltage	--	2.4	5.0	5.5	V
I_{dd1}	Normal Mode Operating Current Typical = (Disable ADC)	Vdd=5V,No GPIO loading IRC Operating , FCPU=8MHz		1.5		mA
	Normal Mode Operating Current Typical = (Disable ADC)	Vddc=3V,No GPIO loading IRC Operating, FCPU=8MHz		1.5		mA
	Normal Mode Operating Current Typical = (Disable ADC)	Vdd=5V,No GPIO loading IRC Operating , FCPU=1MHz		0.5		mA
	Normal Mode Operating Current Typical = (Disable ADC)	Vddc=3V,No GPIO loading IRC Operating, FCPU=1MHz		0.5		mA
I_{dd2}	Slow Mode Operating Current Typical = (Disable ADC)	Vdd=5V,No GPIO loading SIRC Operating, FCPU=32KHz		230		uA
	Slow Mode Operating Current Typical = (Disable ADC)	Vdd=3V,No GPIO loading SIRC Operating, FCPU=32KHz		215		uA
I_{dd3}	Green Mode Operating Current (watch Dog Enable) Typical = (Disable LVDT)	Vdd=5V,No GPIO loading WDT = 32ms, FCPU=Disable SIRC Operating and vary with VDD		25		uA
	Green Mode Operating Current (watch Dog Enable) Typical = (Disable LVDT)	Vdd=5V,No GPIO loading WDT = 32ms, FCPU=Disable SIRC Operating and don't vary with VDD		12		uA
	Green Mode Operating Current (watch Dog Enable) Typical = (Disable LVDT)	Vdd=3V,No GPIO loading WDT = 32ms SIRC Operating ,FCPU=Disable		6		uA

Symbol	Parameter	Conditions	Values			Unit
			MIN.	TYP	MAX	
I_{dd4}	Suspend Mode Current Typical = (Disable ADC)	Vdd=5V,No GPIO loading 25 ℃		1.5	4.0	uA
	Suspend Mode Current Typical = (Disable ADC)	Vdd=3V,No GPIO loading 25 ℃		1	3.0	uA
V_{LVDT}	Low Voltage Detect	VDT36 , △ = 150 mV	3.6-△	3.6	3.6+△	V
		VDT24 , △ = 150 mV	2.4-△	2.4	2.4+△	V
		VDT30 , △ = 150 mV	3.0-△	3.0	3.0+△	V
						V
$V_{POR/PDR}$	Power on Reset/ Power down Reset	Power from 0V to VDD (VIH)(POR)		2.4		V
		Power from VDD to 0V(VIL) (PDR)		2		V
F_{CPU}	MCU clock frequency	25 ℃, VDD > 2.1V			8	MHz
F_{IRC}	Internal high RC frequency	VDD=5V, 25 ℃, F_{IRC}16Mhz △ = 16 * (2%)	16 - △	16	16+△	MHz
		VDD=2.2~5V, @25 ℃ F_{IRC} = 16Mhz △ = 16 * (2 %)	16 - △	16	16+△	MHz
F_{SIRC}	Internal Slow RC frequency	VDD=2.2~5V, @25 ℃ △ = 32 * (10 %)	32 -△	32	32+△	KHz
T_{POREXT}	Power on reset Timing	SELPOR = 2'b11 (64ms) VDD =5V	61		67	mS
		SELPOR = 2'b11 (64ms) VDD =3V	61		67	mS
V_{INREFH}	Internal Reference High	V_{INREFH} = 4V (Vdd=5V,@ 25 ℃) △ = 4V * (2 %)	4-△	4	4+△	V
		V_{INREFH} = 3V (Vdd=5V, @25 ℃) △ = 3V * (2 %)	3-△	3	3+△	V
		V_{INREFH} = 2V(Vdd=5V, @25 ℃) △ = 2V * (2 %)	2-△	2	2+△	V

12.2 GPIO Interface

Symbol	Parameter	Conditions	Values			Unit
			MIN.	TYP.	MAX.	
V_{up1}	GPIO Pull-up Resistor	VDD=5V	90		110	KΩ
V_{up2}	GPIO Pull-up Resistor	VDD=3V	90		110	KΩ
V_{OL}	Output Low Voltage(High drive)	VDD=5~3V , I_{OL}=15mA	-		0.2	V
		VDD=3~2.4, I_{OL}=15mA			0.25	V
V_{OH}	Output High Voltage	VDD=5~3V, I_{OH}=15mA VDD=3V~2.4V, I_{OH}=11mA	VDD-0.4V		-	V
V_{IL}	Input Low Voltage	VDD=5V (All GPIO input)		0.3*VDD		V
		VDD=4V (All GPIO input)		0.3*VDD		V
		VDD=2.2V (All GPIO input)		0.3*VDD		V
V_{IH}	Input High Voltage	VDD=5V (All GPIO input)		0.7*VDD		V
		VDD=4V (All GPIO input)		0.7*VDD		V
		VDD=2.2V (All GPIO input)		0.7*VDD		V
V_{IL2}	Input Low Voltage	Reset Pin				V
V_{OH_vpp}	VPP pin output High	VDD=5~2.4V, I_{OH}=15mA			VDD-0.7V	
V_{OL_vpp}	VPP pin output low	VDD=5~2.4V, I_{OL}<2mA			0.7V	
V_{PH_vpp}	VPP Pull High Voltage	VDD=5V (VPP output)	3.5V		--	V
		VDD=4V (VPP output)	2.6V		--	V
		VDD=2.4V (VPP output)	1.4V		--	V

12.3 ADC specification

Symbol	Parameter	Conditions	Values			Unit
			min.	Typ.	max.	
ADCSR	ADC sample Rate	-			32	KHz
DNL	Differential Nonlinearity	Resolution = 12 bit VDD=5.0V, VREFH = 3.3V FADCSR=32K			--	LSB
		Resolution = 10 bit VDD=5.0V, VREFH = 3.3V FADCSR=32K			--	LSB
INL	Integral Nonlinearity	Resolution = 12 bit VDD=5.0V, VREFH = 3.3V FADCSR=32K			--	LSB
		Resolution = 10 bit VDD=5.0V, VREFH = 3.3V FADCSR=32K			--	LSB
GE	Gain Error	Resolution = 12 bit VDD=5.0V, VREFH = 3.3V FADCSR=32K			--	LSB
		Resolution = 10 bit VDD=5.0V, VREFH = 3.3V FADCSR=32K			--	LSB
ADCRL	ADC Resolution Typical = bit	VDD=5.0V, VREFH = 3.3V FADCSR=32K	8	10	12	bit
ADCRL	ADC Resolution Typical = bit	VDD=5.0V, VREFH = Internal 2V/3V/4V FADCSR=32K	8	9	11	bit
					-	

12.4 CMP specification

Symbol	Parameter	Conditions	Values			Unit
			min.	Typ.	max.	
V_{IO}	Input offset voltage	VDD=5V~2.4V		+/-10		mV
V_{ICM}	Input common mode voltage	VDD=5V~2.4V	0		VDD	V

【13】 Package Diagram

13.1 10-PIN MSOP