EPROM/ROM-Based Remote Controller

Devices Included in this Data Sheet:

- FM8A23E : EPROM device
- FM8A23 : Mask ROM device

FEATURES

- Only 36 single word instructions
- All instructions are single cycle except for program branches which are two-cycle
- 13-bit wide instructions
- All ROM/EPROM area GOTO instruction
- All ROM/EPROM area subroutine CALL instruction
- 8-bit wide data path
- 2-level deep hardware stack
- 512 x 13 bits on chip EPROM/ROM
- 35 x 8 bits on chip general purpose registers (SRAM)
- Operating speed: DC-8 MHz clock input
  DC-250 ns instruction cycle

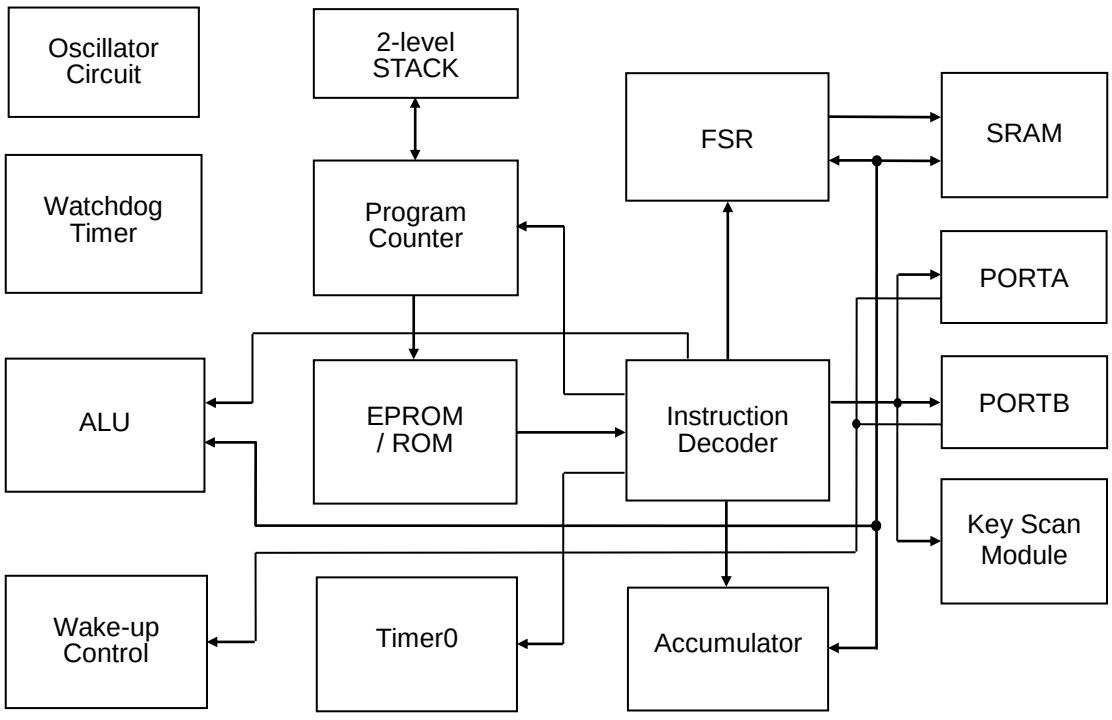
Device	Pins #	I/O #	EPROM/ROM (Word)	RAM (Byte)
FM8A23/A23E	16	12	512	35

- 1 channel IR output with programmable frequency and duty cycle
- Direct, indirect addressing modes for data accessing
- 8-bit real time clock/counter (Timer0) with 8-bit programmable prescaler
- Internal Power-on Reset (POR)
- Built-in Low Voltage Detector (LVD) for Brown-out Reset (BOR)
- Power-up Reset Timer (PWRT) and Oscillator Start-up Timer(OST)
- On chip Watchdog Timer (WDT) with internal oscillator for reliable operation and soft-ware watch-dog enable/disable control
- Two I/O ports IOA and IOB with independent direction control
- Wake-up from SLEEP by Port B input status change
- Power saving SLEEP mode
- Programmable Code Protection
- Selectable oscillator options:
  - ERC: External Resistor/Capacitor Oscillator
  - XT: 455KHz Resonator Oscillator
- Wide-operating voltage range:
  - EPROM : 1.8V to 5.5V
  - ROM : 1.8V to 5.5V

GENERAL DESCRIPTION

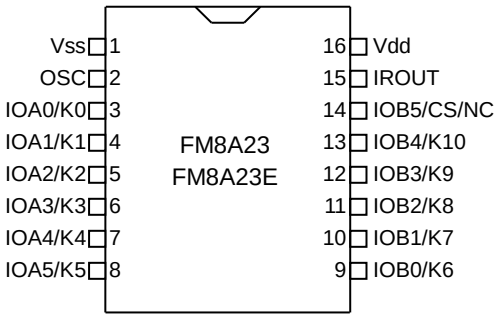
The FM8A23 series is a family of low-cost, high speed, high noise immunity, EPROM/ROM-based 8-bit CMOS microcontrollers. It employs a RISC architecture with only 36 instructions. All instructions are single cycle except for program branches which take two cycles. The easy to use and easy to remember instruction set reduces development time significantly.
The FM8A23 series consists of Power-on Reset (POR), Brown-out Reset (BOR), Power-up Reset Timer (PWRT), Oscillator Start-up Timer(OST), Watchdog Timer, EPROM/ROM, SRAM, tri-state I/O port, Power saving SLEEP mode, real time programmable clock/counter, Wake-up from SLEEP mode, and Code Protection for EPROM products. There are one oscillator configurations to choose from, including the resonator and RC oscillator.
The FM8A23 address 512×13 of program memory.
The FM8A23 can directly or indirectly address its register files and data memory. All special function registers including the program counter are mapped in the data memory.

BLOCK DIAGRAM



PIN CONNECTION

PDIP, SOP



PIN DESCRIPTIONS

Name	I/O	Description
IOA0 ~ IOA5	I/O	Bi-direction I/O pins
IOB0 ~ IOB5	I/O	Bi-direction I/O pins with system wake-up function and **IOB5 is an input only pin**
K0 ~ K10	I/O	Key scan I/O pins
CS	I	Custom code select by connecting Vdd or K0 ~ K10
NC	-	No connection
IROUT	O	IR carrier output pin
OSC	I	For 455 KHz resonator oscillator
Vdd	-	Positive supply
Vss	-	Ground

Legend: I=input, O=output, I/O=input/output

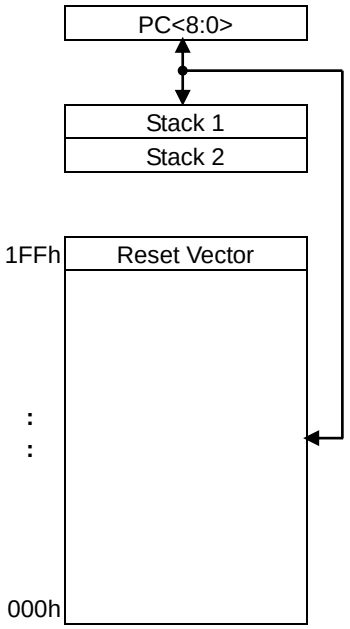
1.0 MEMORY ORGANIZATION

FM8A23 memory is organized into program memory and data memory.

1.1 Program Memory Organization

The FM8A23 have a 9-bit Program Counter (PC) capable of addressing a 512×13 program memory space.
The RESET vector for the FM8A23 is at 1FFh.
FM8A23 supports all ROM/EPROM area **CALL**/**GOTO** instructions without page.

FIGURE 1.1: Program Memory Map and STACK



FM8A23/23E

1.2 Data Memory Organization

Data memory is composed of Special Function Registers and General Purpose Registers.
The General Purpose Registers are accessed either directly or indirectly through the FSR register.
The Special Function Registers are registers used by the CPU and peripheral functions to control the operation of the device.

TABLE 1.1: Registers File Map for FM8A23/23E Series

Address	Description
00h	INDF
01h	TMR0
02h	PCL
03h	STATUS
04h	FSR
05h	PORTA
06h	PORTB
07h	CHIPCON
08h	General Purpose Register
09h	General Purpose Register
0Ah	General Purpose Register
0Bh	WUCON
0Ch	IRCYCLE
0Dh	IRDUTY
0Eh	KEYDATA
0Fh	CSDATA
10h | 2Fh	General Purpose Registers

NA	OPTION
05h	IOSTA
06h	IOSTB

TABLE 1.3: Operational Registers Map

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
00h (r/w)	INDF	Uses contents of FSR to address data memory (not a physical register)							
01h (r/w)	TMR0	8-bit real-time clock/counter							
02h (r/w)	PCL	Low order 8 bits of PC							
03h (r/w)	STATUS	GP2	GP1	GP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C
04h (r/w)	FSR	*	*	Indirect data memory address pointer					
05h (r/w)	PORTA	-	-	IOA5	IOA4	IOA3	IOA2	IOA1	IOA0
06h (r/w)	PORTB	-	-	IOB5	IOB4	IOB3	IOB2	IOB1	IOB0
07h (r/w)	CHIPCON	WDTE	LVDTE	-	-	KEYON	IROEN	-	IREN
0Bh (w)	WUCON	-	-	WUB5	WUB4	WUB3	WUB2	WUB1	WUB0
0Ch (w)	IRCYCLE	IRC7	IRC6	IRC5	IRC4	IRC3	IRC2	IRC1	IRC0
0Dh (w)	IRDUTY	IRD7	IRD6	IRD5	IRD4	IRD3	IRD2	IRD1	IRD0
0Eh (r)	KEYDATA	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0
0Fh (r)	CSDATA	-	-	-	-	CD3	CD2	CD1	CD0

Legend: - = unimplemented, read as '0', * = unimplemented, read as '1'

TABLE 1.2: The Registers Controlled by OPTION or IOST Instructions

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
N/A (w)	OPTION			T0CS	T0SE	PSA	PS2	PS1	PS0
05h (w)	IOSTA			Port A I/O Control Register					
06h (w)	IOSTB			Port B I/O Control Register					

2.0 FUNCTIONAL DESCRIPTIONS

2.1 Operational Registers

2.1.1 INDF (Indirect Addressing Register)

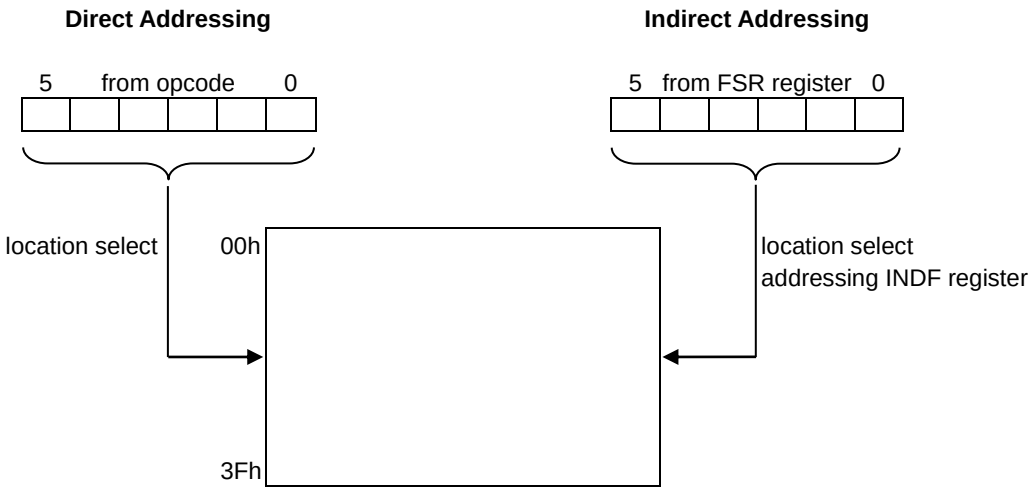
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
00h (r/w)	INDF	Uses contents of FSR to address data memory (not a physical register)							

The INDF Register is not a physical register. Any instruction accessing the INDF register can actually access the register pointed by FSR Register. Reading the INDF register itself indirectly (FSR="0") will read 00h. Writing to the INDF register indirectly results in a no-operation (although status bits may be affected).
The bits 5-0 of FSR register are used to select up to 64 registers (address: 00h ~ 3Fh).

EXAMPLE 2.1: INDIRECT ADDRESSING

- Register file 38 contains the value 10h
- Register file 39 contains the value 0Ah
- Load the value 38 into the FSR Register
- A read of the INDF Register will return the value of 10h
- Increment the value of the FSR Register by one (@FSR=39h)
- A read of the INDR register now will return the value of 0Ah.

FIGURE 2.1: Direct/Indirect Addressing for FM8A23/23E



2.1.2 TMR0 (Time Clock/Counter register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
01h (r/w)	TMR0	8-bit real-time clock/counter							

The Timer0 is an 8-bit timer/counter. The clock source of Timer0 can come from the instruction cycle clock or by an internal IROUT carrier clock defined by T0CS bit (OPTION<5>). If internal IROUT carrier clock is selected, the Timer0 is increased by internal IROUT carrier clock rising/falling edge (selected by T0SE bit (OPTION<4>)).
The prescaler is assigned to Timer0 by clearing the PSA bit (OPTION<3>). In this case, the prescaler will be cleared when TMR0 register is written with a value.

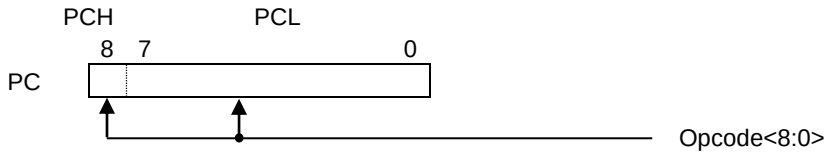
2.1.3 PCL (Low Bytes of Program Counter) & Stack

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
02h (r/w)	PCL	Low order 8 bits of PC							

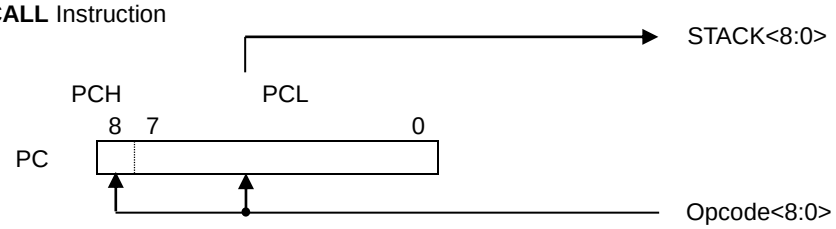
FM8A23 devices have a 9-bit wide Program Counter (PC) and two-level deep 9-bit hardware push/pop stack. The low byte of PC is called the PCL register and which contains the PC<7:0> bits. This register is readable and writable. The high byte of PC is called the PCH register. This register contains the PC<8> bit and is not directly readable or writable. As a program instruction is executed, the Program Counter will contain the address of the next program instruction to be executed. The PC value is increased by one, every instruction cycle, unless an instruction changes the PC.
For a GOTO instruction, the PC<8:0> is provided by the GOTO instruction word. The PCL register is mapped to PC<7:0>.
For a CALL instruction, the PC<8:0> is provided by the CALL instruction word. The next PC will be loaded (PUSHed) onto the top of STACK. The PCL register is mapped to PC<7:0>.
For a RETIA, or RETURN instruction, the PC are updated (POPed) from the top of STACK. The PCL register is mapped to PC<7:0>.
For any instruction where the PCL is the destination, the PC<7:0> is provided by the instruction word or ALU result. However, the PC<8> will be cleared to “0”.

FIGURE 2.2: Loading of PC in Different Situations

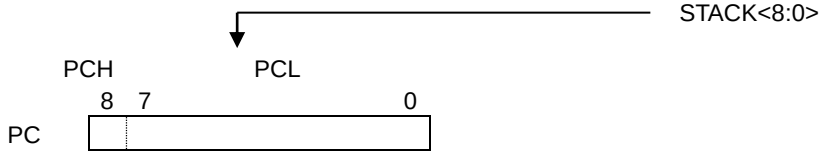
Situation 1: **GOTO** Instruction



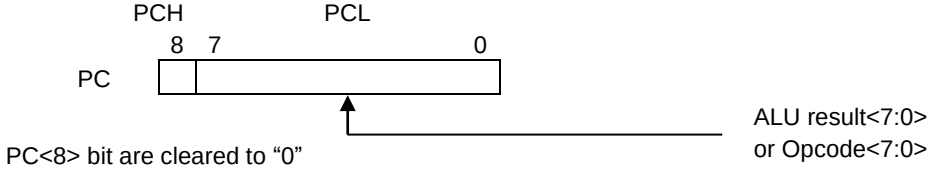
Situation 2: **CALL** Instruction



Situation 3: **RETIA**, or **RETURN** Instruction



Situation 4: Instruction with PCL as destination



2.1.4 STATUS (Status Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
03h (r/w)	STATUS	GP2	GP1	GP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C

This register contains the arithmetic status of the ALU, the RESET status.
If the STATUS Register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS Register as destination may be different than intended. For example, CLRR STATUS will clear the upper three bits and set the Z bit. This leaves the STATUS Register as 000u u1uu (where u = unchanged).

C : Carry/borrow bit.
ADDAR, ADDIA
= 1, a carry occurred.
= 0, a carry did not occur.
SUBAR, SUBIA
= 1, a borrow did not occur.
= 0, a borrow occurred.
Note : A subtraction is executed by adding the two's complement of the second operand. For rotate (RRR, RLR) instructions, this bit is loaded with either the high or low order bit of the source register.

DC : Half carry/half borrow bit.
ADDAR, ADDIA
= 1, a carry from the 4th low order bit of the result occurred.
= 0, a carry from the 4th low order bit of the result did not occur.
SUBAR, SUBIA
= 1, a borrow from the 4th low order bit of the result did not occur.
= 0, a borrow from the 4th low order bit of the result occurred.

Z : Zero bit.
= 1, the result of a logic operation is zero.
= 0, the result of a logic operation is not zero.

$\overline{PD}$: Power down flag bit.
= 1, after power-up or by the CLRWDT instruction.
= 0, by the SLEEP instruction.

$\overline{TO}$: Time overflow flag bit.
= 1, after power-up or by the CLRWDT or SLEEP instruction.
= 0, a watch-dog time overflow occurred.

GP2:GP0 : General purpose read/write bits.

2.1.5 FSR (Indirect Data Memory Address Pointer)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
04h (r/w)	FSR	*	*	Indirect data memory address pointer					

Bit5:Bit0 : Select registers address in the indirect addressing mode. See 2.1.1 for detail description.

Bit7:6 : Not used. Read as “1”s.

2.1.6 PORTA & PORTB (Port Data Registers)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
05h (r/w)	PORTA	-	-	IOA5	IOA4	IOA3	IOA2	IOA1	IOA0
06h (r/w)	PORTB	-	-	IOB5	IOB4	IOB3	IOB2	IOB1	IOB0

Both PORTA and PORTB are 6-bit port data registers. Only the low order 6 bits are used (PORTA<5:0> & PORTB<5:0>). Reading the port (PORTA, PORTB register) reads the status of the pins independent of the pin’s input/output modes. Bits 7-6 of PORTA and PORTB are unimplemented and read as ‘0’s. And IOB5 is an input pin only.
Writing to these ports will write to the port data latch.

2.1.7 CHIPCON (Chip Control Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
07h (r/w)	CHIPCON	WDTE	LVDTE	-	-	KEYON	IROEN	-	IREN

IREN : IROUT module enable bit.
= 0, IROUT module is disabled (IROUT carrier generator is off).
= 1, IROUT module is enabled (IROUT carrier generator is on).

Bit1 : Not used. Read as “0”.

IROEN : IROUT carrier output enable bit.
= 0, IROUT carrier output is disabled.
= 1, IROUT carrier output is enabled.

Bit5:4 : Not used. Read as “0”s.

KEYON : H/W Key scan enable bit which is valid only on IOSEL = 0 (T-type keyboard mode).
= 0, H/W Key scan is disabled.
= 1, H/W Key scan is enabled.

LVDTE : LVDT (low voltage detector) enable bit.
= 0, Disable LVDT.
= 1, Enable LVDT.

WDTE : WDT (watch-dog timer) enable bit.
= 0, Disable WDT.
= 1, Enable WDT.

2.1.8 WUCON (Port B Input Change Wake-up Control Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0Bh (w)	WUCON	-	-	WUB5	WUB4	WUB3	WUB2	WUB1	WUB0

WUB0 : = 1, Enable the input falling wake-up function of IOB0 pin.
= 0, Disable the input falling wake-up function of IOB0 pin.

WUB1 : = 1, Enable the input falling wake-up function of IOB1 pin.
= 0, Disable the input falling wake-up function of IOB1 pin.

WUB2 : = 1, Enable the input falling wake-up function of IOB2 pin.
= 0, Disable the input falling wake-up function of IOB2 pin.

WUB3 : = 1, Enable the input falling wake-up function of IOB3 pin.
= 0, Disable the input falling wake-up function of IOB3 pin.

WUB4 : = 1, Enable the input falling wake-up function of IOB4 pin.
= 0, Disable the input falling wake-up function of IOB4 pin.

WUB5 : = 1, Enable the input falling wake-up function of IOB5 pin.
= 0, Disable the input falling wake-up function of IOB5 pin.

Bit7:6 : Not used.

2.1.9 IRCYCLE (IROUT Cycle Control Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0Ch (w)	IRCYCLE	IRC7	IRC6	IRC5	IRC4	IRC3	IRC2	IRC1	IRC0

IRC7:IRC0 : IROUT (IR Carrier output) frequency = (Oscillator frequency) / (IRC7:IRC0).

2.1.10 IRDUTY (IROUT Duty Control Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0Dh (w)	IRDUTY	IRD7	IRD6	IRD5	IRD4	IRD3	IRD2	IRD1	IRD0

IRD7:IRD0 : IROUT (IR Carrier output) duty cycle = (IRD7:IRD0) / (IRC7:IRC0).
(IRD7:IRD0) must be less than (IRC7:IRC0).

2.1.11 KEYDATA (Key-Pressed Information Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0Eh (r)	KEYDATA	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0

KD7:KD0 : Key-pressed Information bits. Used only for T-type keyboard. See FIGURE 2.3 for detail description.
= 00h, K0-K1 key is pressed.
= 01h, K0-K2 key is pressed.
|
= 40h, K9-Vss key is pressed.
= 41h, K10-Vss key is pressed.
= FFh, no key is pressed.

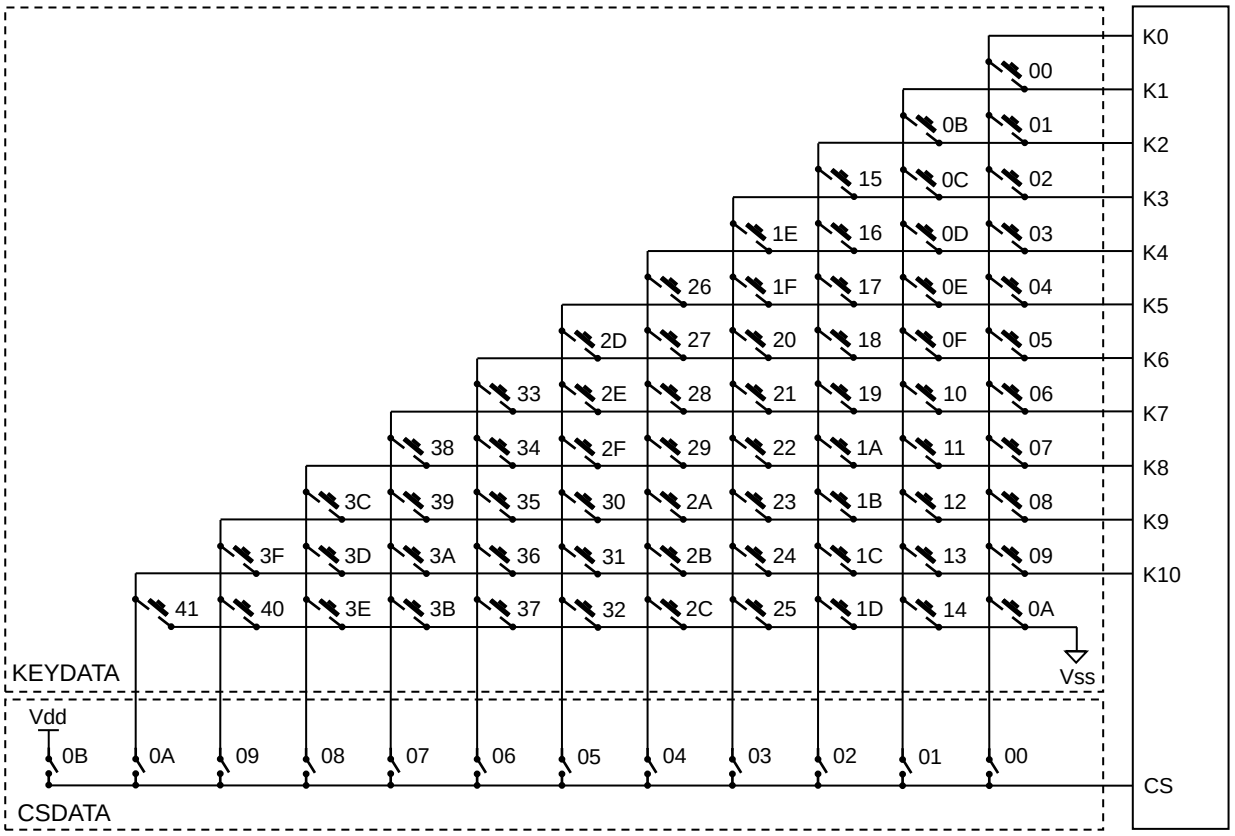
2.1.12 CSDATA (Custom Code Selection Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0Fh (r)	CSDATA	-	-	-	-	CD3	CD2	CD1	CD0

CD3:CD0 : Custom code select bits. Used only for T-type keyboard. See FIGURE 2.3 for detail description.
= 00, CS pin is connected to K0 pin.
= 01, CS pin is connected to K1 pin.
= 02, CS pin is connected to K2 pin.
|
= 09, CS pin is connected to K9 pin.
= 0A, CS pin is connected to K10 pin.
= 0B, CS pin is connected to Vdd pin.

Bit7:4 : Not used. Read as “0”s.

FIGURE 2.3: KEYDATA & CSDATA Selection



2.1.13 ACC (Accumulator)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
N/A (r/w)	ACC	Accumulator							

Accumulator is an internal data transfer, or instruction operand holding. It can not be addressed.

2.1.14 OPTION Register

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
N/A (w)	OPTION			T0CS	T0SE	PSA	PS2	PS1	PS0

Accessed by OPTION instruction.

By executing the OPTION instruction, the contents of the ACC Register will be transferred to the OPTION Register. The OPTION Register is a 7-bit wide, write-only register which contains various control bits to configure the Timer0/WDT prescaler, and Timer0.
The OPTION Register are “write-only” and are set all “1.

PS2:PS0 : Prescaler rate select bits.

PS2:PS0	Timer0 Rate	WDT Rate
0 0 0	1:2	1:1
0 0 1	1:4	1:2
0 1 0	1:8	1:4
0 1 1	1:16	1:8
1 0 0	1:32	1:16
1 0 1	1:64	1:32
1 1 0	1:128	1:64
1 1 1	1:256	1:128

PSA : Prescaler assign bit.
= 1, WDT (watch-dog timer).
= 0, TMR0 (Timer0).

T0SE : TMR0 source edge select bit.
= 1, Falling edge on internal IROUT carrier clock.
= 0, Rising edge on internal IROUT carrier clock.

T0CS : TMR0 clock source select bit.
= 1 → Internal IROUT carrier clock.
= 0 → Internal instruction clock cycle.

Bit7:6 : Not used.

2.1.15 IOSTA & IOSTB (Port I/O Control Registers)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
05h (w)	IOSTA			Port A I/O Control Register					
06h (w)	IOSTB			Port B I/O Control Register					

Accessed by IOST instruction.

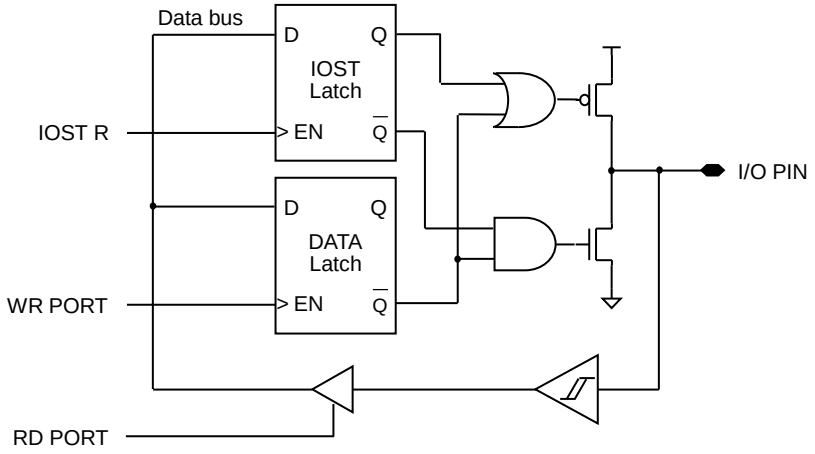
The Port I/O Control Registers are loaded with the contents of the ACC Register by executing the IOST R (05h~06h) instruction. A ‘1’ from a IOST Register bit puts the corresponding output driver in hi-impedance state (input mode). A ‘0’ enables the output buffer and puts the contents of the output data latch on the selected pins (output mode). The IOST Registers are “write-only” and are set (output drivers disabled) upon RESET.

2.2 I/O Ports

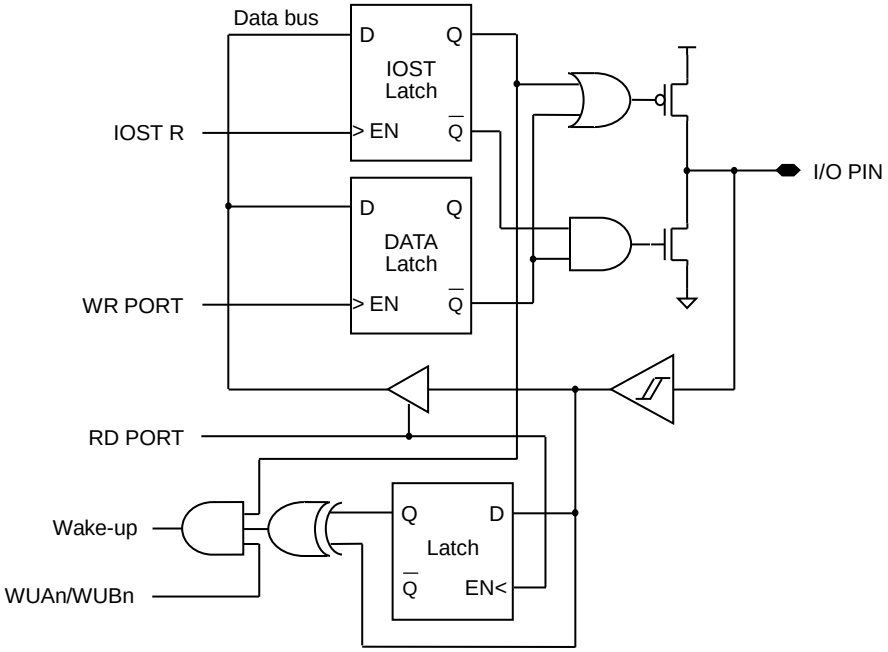
Port A and port B are bi-directional tri-state I/O ports. Both Port A and Port B are 6-pin I/O ports. Please note that IOB5 is an input pin only.
All I/O pins (IOA<5:0> and IOB<5:0>) have data direction control registers (IOSTA and IOSTB) which can configure these pins as output or input. The exception is IOB5 which is input only.
All of IOB<5:0> also provide the input change wake-up function. Each pin has its corresponding input change wake-up enable bits (WUCON registers) to select the input change wake-up source.

FIGURE 2.4: Block Diagram of I/O PINs

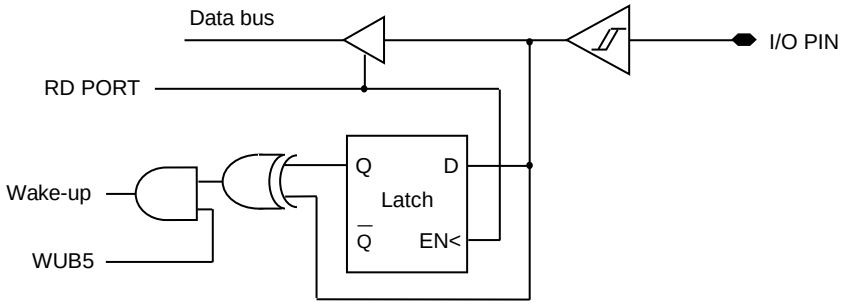
IOA0 ~ IOA5 :



IOB0 ~ IOB4 :



IOB5 :



2.3 Timer0/WDT & Prescler

2.3.1 Timer0

The Timer0 is a 8-bit timer/counter. The clock source of Timer0 can come from the internal clock, or by an internal IROUT carrier clock.

2.3.1.1 Using Timer0 with an Internal Clock : Timer mode

Timer mode is selected by clearing the T0CS bit (OPTION<5>). In timer mode, the timer0 register (TMR0) will increment every instruction cycle (without prescaler). If TMR0 register is written, the increment is inhibited for the following two cycles.

2.3.1.2 Using Timer0 with an IROUT Carrier Clock : Counter mode

Counter mode is selected by clearing the T0CS bit (OPTON<5>). In this mode, Timer0 will increment either on every rising or falling edge of internal IROUT carrier clock. The incrementing edge is determined by the source edge select bit T0SE (OPTION<4>).
The IROUT clock requirement is due to internal phase clock (Tosc) synchronization. Also, there is a delay in the actual incrementing of Timer0 after synchronization.
When no prescaler is used, the IROUT clock input is the same as the prescaler output. The synchronization of IROUT clock with the internal phase clocks is accomplished by sampling the prescaler output on the T2 and T4 cycles of the internal phase clocks. Therefore, it is necessary for IROUT carrier clock to be high for at least 2 T_{OSC} and low for at least 2 Tosc.
When a prescaler is used, the IROUT carrier clock input is divided by the asynchronous prescaler. For the IROUT clock to meet the sampling requirement, the ripple counter must be taken into account. Therefore, it is necessary for IROUT carrier clock input to have a period of at least 4Tosc divided by the prescaler value.

2.3.2 Watchdog Timer (WDT)

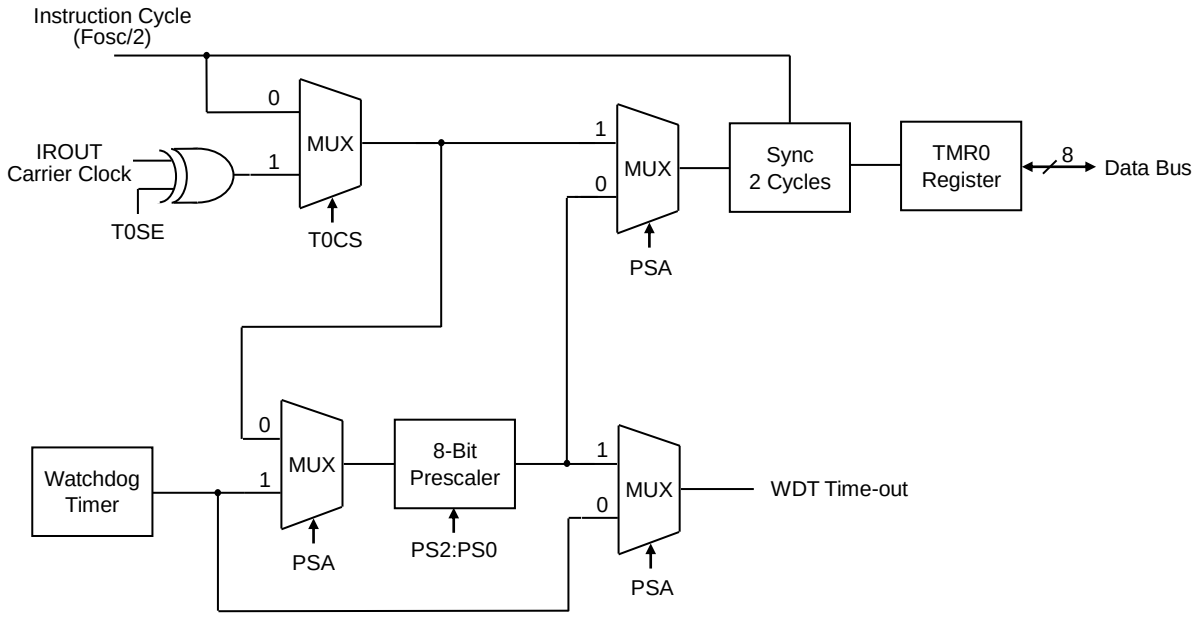
The Watchdog Timer (WDT) is a free running on-chip RC oscillator which does not require any external components. So the WDT will still run even if the clock on the OSCI and OSCO pins is turned off, such as in SLEEP mode. During normal operation or in SLEEP mode, a WDT time-out will cause the device reset and the $\overline{TO}$ bit (STATUS<4>) will be cleared.
The WDT can be disabled by clearing the control bit WDTE (CHIPCON<7>) to “0”.
The WDT has a nominal time-out period of 20 ms (without prescaler). If a longer time-out period is desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT controlled by the OPTION register. Thus, the longest time-out period is approximately 2.6 seconds.

The CLRWDT instruction clears the WDT and the prescaler, if assigned to the WDT, and prevents it from timing out and generating a device reset.
The SLEEP instruction resets the WDT and the prescaler, if assigned to the WDT. This gives the maximum SLEEP time before a WDT Wake-up Reset.

2.3.3 Prescaler

An 8-bit counter (down counter) is available as a prescaler for the Timer0, or as a postscaler for the Watchdog Timer (WDT). Note that the prescaler may be used by either the Timer0 module or the WDT, but not both. Thus, a prescaler assignment for the Timer0 means that there is no prescaler for the WDT, and vice-versa.
The PSA bit (OPTION<3>) determines prescaler assignment. The PS<2:0> bits (OPTION<2:0>) determine prescaler ratio.
When the prescaler is assigned to the Timer0 module, all instructions writing to the TMR0 register will clear the prescaler. When it is assigned to WDT, a CLRWDT instruction will clear the prescaler along with the WDT.
The prescaler is neither readable nor writable. On a RESET, the prescaler contains all '1's.
To avoid an unintended device reset, CLRWDT or CLRR TMR0 instructions must be executed when changing the prescaler assignment from Timer0 to the WDT, and vice-versa.

FIGURE 2.5: Block Diagram of The Timer0/WDT Prescaler



2.4 IR Carrier Output (IROUT)

FM8A23 is build-in an IR carrier output generator. The output is controlled by IROEN (CHIPCON<2>), IREN (CHIPCON<0>) bits and IRCYCLE, IRDUTY registers.
The IROUT frequency and duty cycle are following the equations below:

IROUT frequency = (Oscillator frequency) / IRCYCLE<7:0>
IROUT duty cycle = IRDUTY<7:0> / IRCYCLE<7:0>

For example, if oscillator frequency is equal to 455KHz, and the IRCYCLE = 12, and IRDUTY = 6, then
IROUT frequency = 455KHz / 12 = 38KHz, and
IROUT duty cycle = 6 / 12 = 50%

Note: The value of IRDUTY<7:0> must be less than IRCYCLE<7:0>.

FIGURE 2.6: IROUT Waveform with Positive Pulse

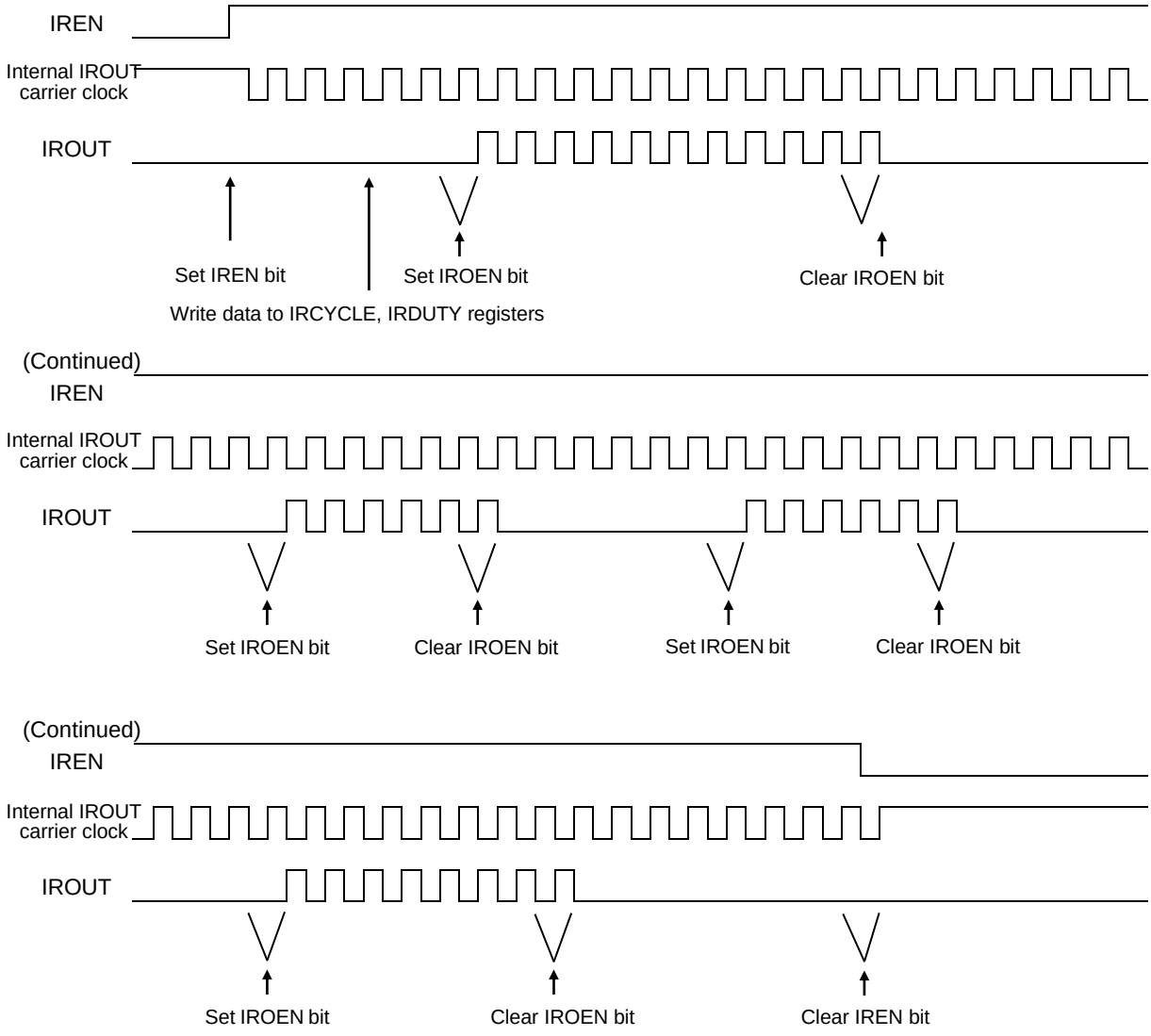
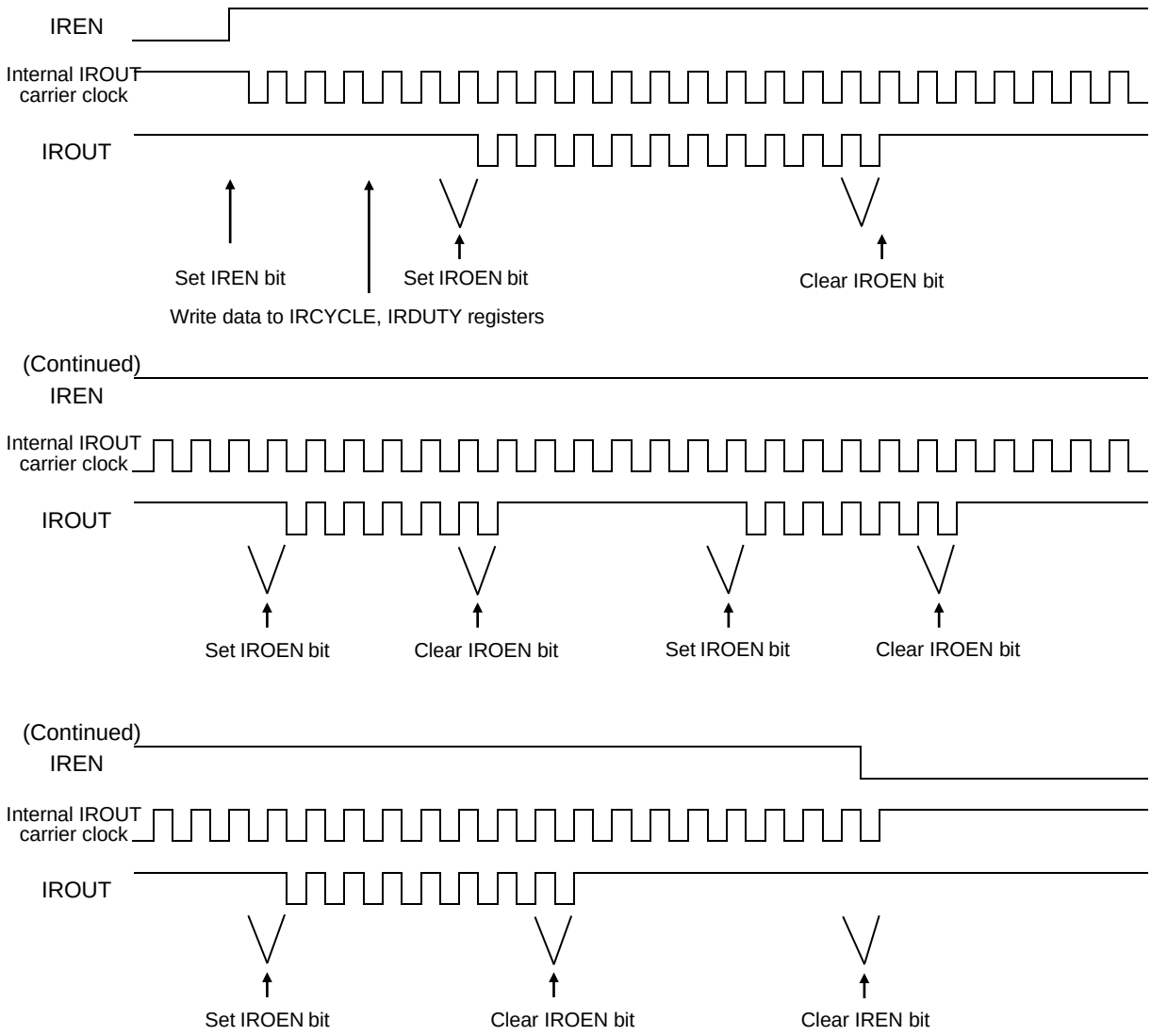


FIGURE 2.7: IROUT Waveform with Negative Pulse



2.6 Power-down Mode (SLEEP)

Power-down mode is entered by executing a SLEEP instruction.
When SLEEP instruction is executed, the $\overline{PD}$ bit (STATUS<3>) is cleared, the $\overline{TO}$ bit is set, the watchdog timer will be cleared and keeps running, and the oscillator driver is turned off.
All I/O pins maintain the status they had before the SLEEP instruction was executed.
To save the power consumption, if the low voltage detector (LVDT) is enabled, user can disable the LVDT by clearing the control bit LVDTE (CHIPCON<6>) before entering into SLEEP mode.

2.6.1 Wake-up from SLEEP Mode

The device can wake-up from SLEEP mode through one of the following events:
1. WDT time-out reset (if enabled).
2. PORTB input status change (used for I/O function or M-type keyboard).
3. Any key-pressed (used for T-type keyboard).

The WDT time-out reset will cause a device reset. The $\overline{PD}$ and $\overline{TO}$ bits can be used to determine the cause of device reset. The $\overline{PD}$ bit is set on power-up and is cleared when SLEEP instruction is executed. The $\overline{TO}$ bit is cleared if a WDT time-out occurred.
For the device to wake-up through a PORTB input status changing event, the program will execute next PC after wake-up. Before entering SLEEP mode, reading PORTB (any instruction accessed to PORTB, including read/write instructions) is necessary. Any pin which corresponding WUBn bit (WUCON<5:0>) is cleared to “0” or configured as output will be excluded from this function.
For the device to wake-up through a key-pressed event, the program will execute next PC after wake-up.
The system wake-up delay time is 20ms plus 128 oscillator cycles time.

2.7 Reset

FM8A23 devices may be RESET in one of the following ways:
1. Power-on Reset (POR)
2. Brown-out Reset (BOR)
3. WDT time-out Reset

Some registers are not affected in any RESET condition. Their status is unknown on Power-on Reset and unchanged in any other RESET. Most other registers are reset to a “reset state” on Power-on Reset or WDT Reset.
A Power-on RESET pulse is generated on-chip when Vdd rise is detected.
On-chip Low Voltage Detector (LVD) places the device into reset when Vdd is below a fixed voltage. This ensures that the device does not continue program execution outside the valid operation Vdd range. Brown-out RESET is typically used in AC line or heavy loads switched applications.
The WDT Wake-up from SLEEP also results in a device RESET, and not a continuation of operation before SLEEP. The $\overline{TO}$ and $\overline{PD}$ bits (STATUS<4:3>) are set or cleared depending on the different reset conditions.

2.7.1 Power-up Reset Timer(PWRT)

The Power-up Reset Timer provides a nominal 20ms delay after Power-on Reset (POR), Brown-out Reset (BOR) or WDT time-out Reset. The device is kept in reset state as long as the PWRT is active.
The PWDT delay will vary from device to device due to Vdd, temperature, and process variation.

2.7.2 Oscillator Start-up Timer(OST)

The OST timer provides a 128 oscillator cycles delay (from OSCI input) after the PWRT delay (20ms) is over. This delay ensures that the X'tal oscillator or resonator has started and stabilized. The device is kept in reset state as long as the OST is active.
This counter only starts incrementing after the amplitude of the OSCI signal reaches the oscillator input thresholds.

2.7.3 Reset Sequence

When Power-on Reset (POR), Brown-out Reset (BOR) or WDT time-out Reset is detected, the reset sequence is as follows:

1. The reset latch is set and the PWRT & OST are cleared.
2. When the internal POR, BOR or WDT time-out Reset pulse is finished, then the PWRT begins counting.
3. After the PWRT time-out, the OST is activated.
4. And after the OST delay is over, the reset latch will be cleared and thus end the on-chip reset signal.

The totally system reset delay time is 20ms plus 128 oscillator cycle time.

FIGURE 2.8: Simplified Block Diagram of on-chip Reset Circuit

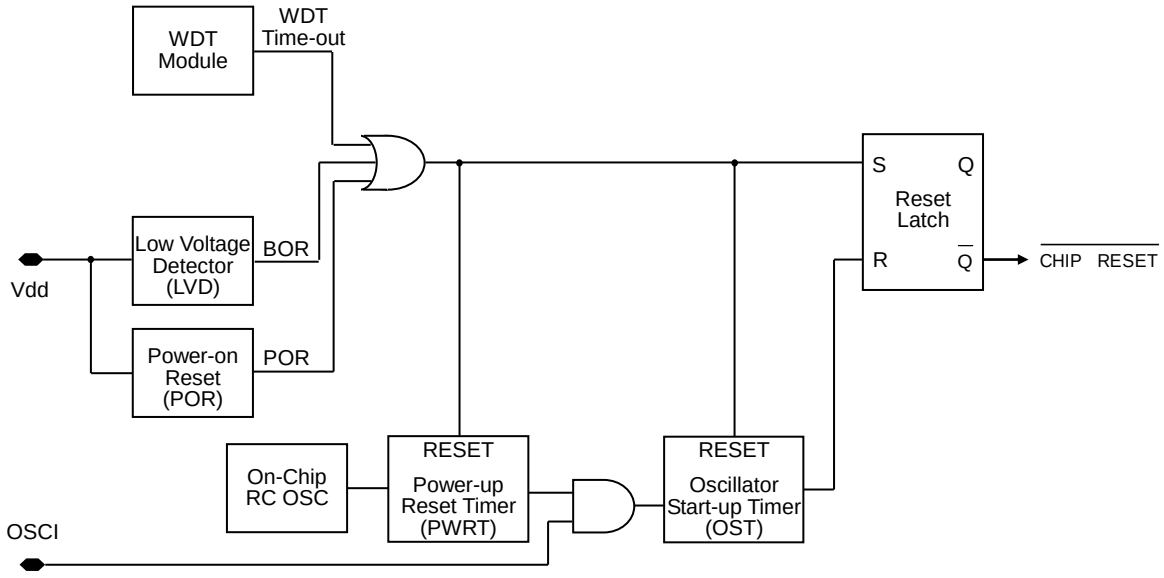


TABLE 2.2: Reset Conditions for All Registers

Register	Address	Power-on Reset Brown-out Reset	WDT Reset
ACC	N/A	xxxx xxxx	uuuu uuuu
OPTION	N/A	--11 1111	--11 1111
IOSTA	05h	--11 1111	--11 1111
IOSTB	06h	--11 1111	--11 1111
INDF	00h	xxxx xxxx	uuuu uuuu
TMR0	01h	xxxx xxxx	uuuu uuuu
PCL	02h	1111 1111	1111 1111
STATUS	03h	0001 1xxx	000# #uuu
FSR	04h	11xx xxxx	11uu uuuu
PORTA	05h	---- xxxx	---- uuuu
PORTB	06h	xxxx xxxx	uuuu uuuu
CHIPCON	07h	11-- 10-0	11-- 10-0
General Purpose Registers	08h ~ 0Ah	xxxx xxxx	uuuu uuuu
WUCON	0Bh	--00 0000	--00 0000
IRCYCLE	0Ch	0000 1100	0000 1100
IRDUTY	0Dh	0000 0110	0000 0110
KEYDATA	0Eh	1111 1111	1111 1111
CSDATA	0Fh	---- 1011	---- 1011
General Purpose Registers	10h ~ 2Fh	xxxx xxxx	uuuu uuuu

Legend: u = unchanged, x = unknown, - = unimplemented,
= refer to the following table for possible values.

TABLE 2.3: $\overline{TO}$ / $\overline{PD}$ Status after Reset

$\overline{TO}$	$\overline{PD}$	RESET was caused by
1	1	Power-on Reset
1	1	Brown-out reset
0	1	WDT Reset during normal operation
0	0	WDT Reset during SLEEP

Legend: u = unchanged

TABLE 2.4: Events Affecting $\overline{TO}$ / $\overline{PD}$ Status Bits

Event	$\overline{TO}$	$\overline{PD}$
Power-on	1	1
WDT Time-Out	0	u
SLEEP instruction	1	0
CLRWDT instruction	1	1

Legend: u = unchanged

2.8 Oscillator Configurations

FM8A23 can be operated in two different oscillator modes. Users can program configuration bit Fosc to select the appropriate modes:

- ERC: External Resistor/Capacitor Oscillator
- XT: 455KHz Resonator Oscillator

In XT mode, a 455KHz ceramic resonator is connected to the OSC and Vss pins to establish oscillation.
The ERC device option offers additional cost savings for timing insensitive applications. The RC oscillator frequency is a function of the supply voltage, the resistor (Rext) and capacitor (Cext), the operating temperature, and the process parameter.

FIGURE 2.9: XT Oscillator Mode (Ceramic Resonator)

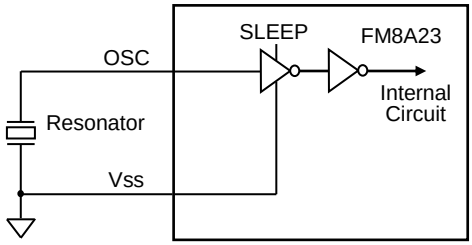
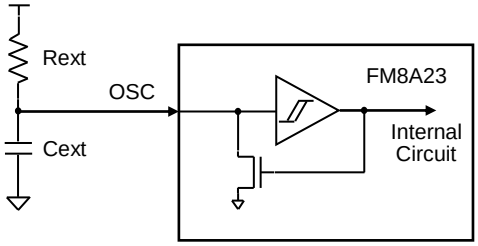


FIGURE 2.10: ERC Oscillator Mode



2.9 Configurations Word

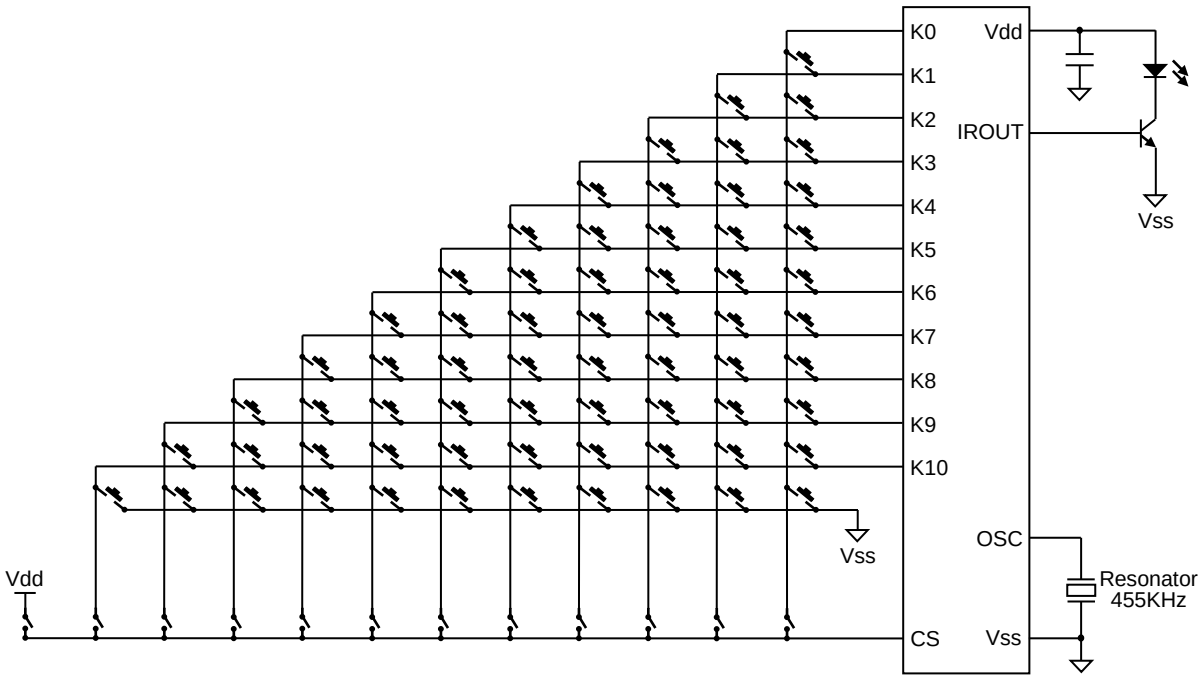
TABLE 2.5: Configurations Word

Name	Description
Fosc	Oscillator Selection Bits = 1 → ERC mode (external R & C) (default) = 0 → XT mode
WDTEN	Watchdog Timer Enable Bit = 1, WDT enabled (default) = 0, WDT disabled
PROTECT	Code Protection Bit = 1, EPROM code protection off (default) = 0, EPROM code protection on
LVDTEN	Low Voltage Detector Enable Bit = 1, Enable, LVDT voltage = 1.8V (default) = 0, Disable (default)
PAPH	Port A internal pull-high Enable Bit = 1, Disable (default) = 0, Enable
PBPH	Port B internal pull-high Enable Bit = 1, Disable (default) = 0, Enable
IRPOL	IROUT Polarity Selection Bit = 1, Negative pulse (without external transistor) (default) = 0, Positive pulse (with external transistor)
IOSEL	[K0 ~ K10, CS] or [IOA5:0, IOB<5:0>] Function Selection Bit = 1, [IOA5:0, IOB<5:0>] pins are selected. Key scan works by S/W. Used for M-type keyboard. = 0, [K0 ~ K10, CS] pins are selected. Key scan works automatically by H/W. Used for T-type keyboard.
CSEN	IOB5/CS/NC Pin Function Enable Bit = 1, IOB5/CS pin works as a NC pin (default) = 0, IOB5/CS pin function is enabled

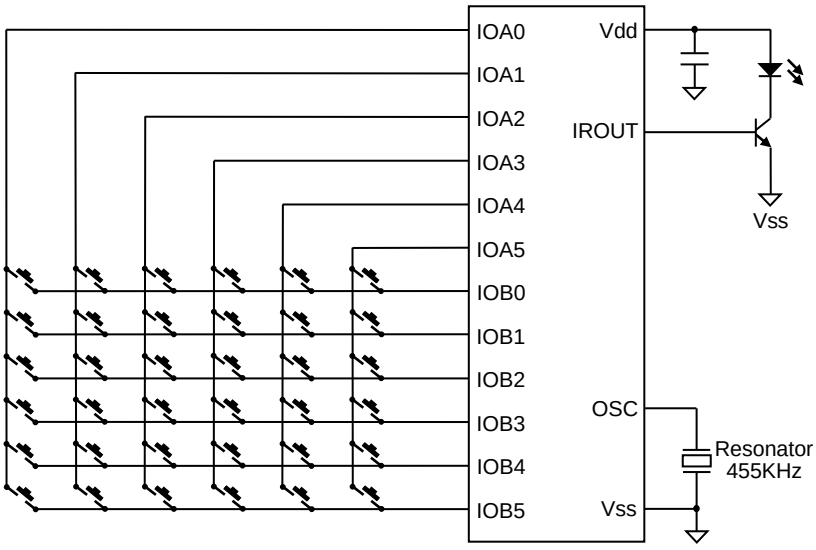
2.10 Application Circuits

2.10.1 IRPOL = 0; Positive Pulse (with External Transistor)

T-Type Keyboard

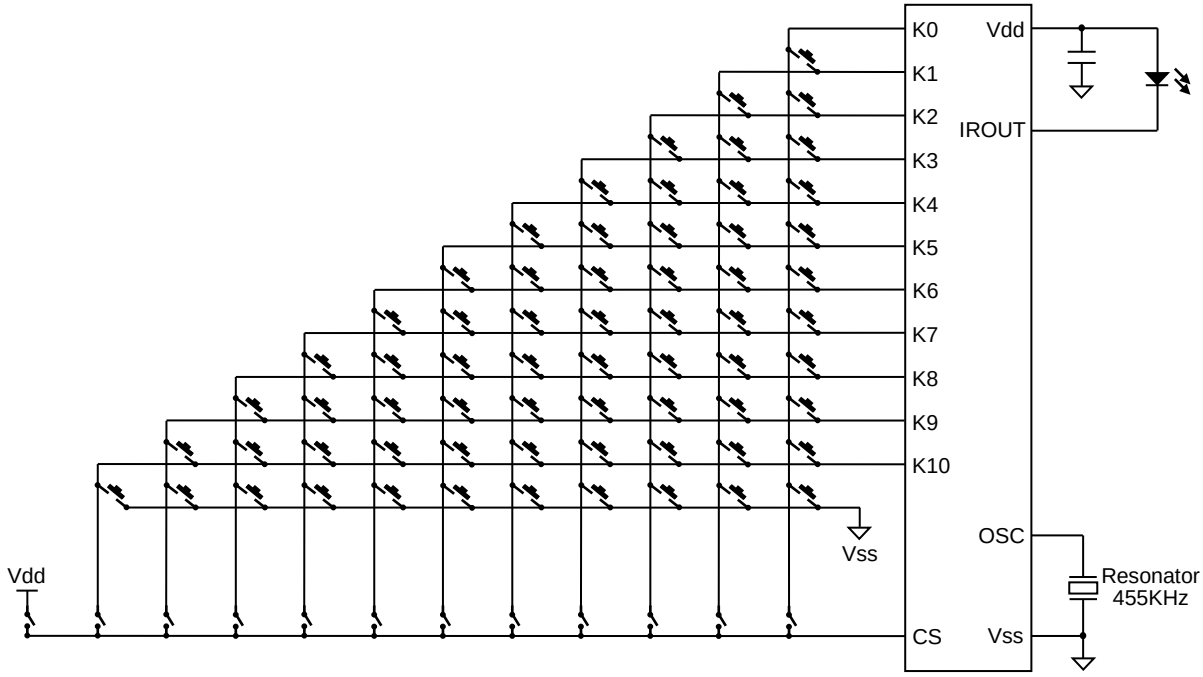


M-Type Keyboard

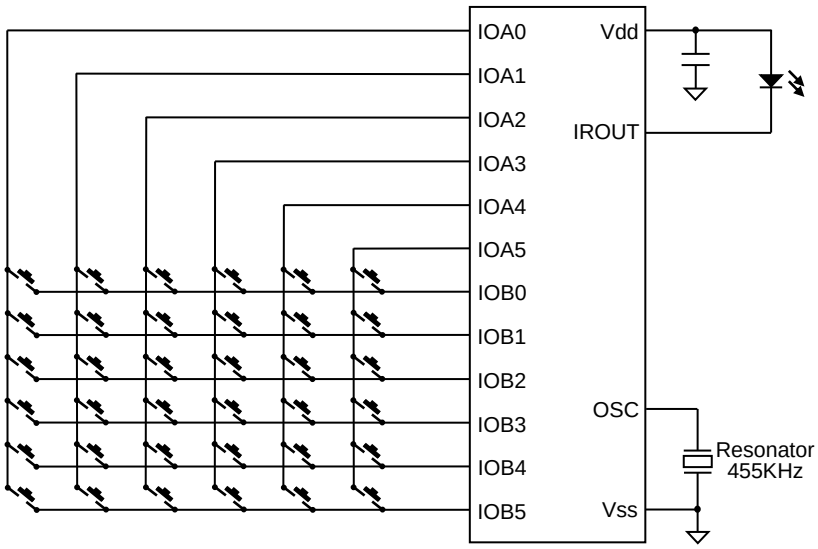


2.10.2 IRPOL = 1; Negative Pulse (without External Transistor)

T-Type Keyboard



M-Type Keyboard



3.0 INSTRUCTION SET

Mnemonic, Operands		Description	Operation	Cycles	Status Affected
BCR	**R, bit**	Clear bit in R	0 → R<b>	1	-
BSR	**R, bit**	Set bit in R	1 → R<b>	1	-
BTRSC	**R, bit**	Test bit in R, Skip if Clear	Skip if R<b> = 0	1/2	-
BTRSS	**R, bit**	Test bit in R, Skip if Set	Skip if R<b> = 1	1/2	-
NOP		No Operation	No operation	1	-
CLRWDT		Clear Watchdog Timer	00h → WDT, 00h → WDT prescaler	1	$\overline{TO}$, $\overline{PD}$
OPTION		Load OPTION register	ACC → OPTION	1	-
SLEEP		Go into power-down mode	00h → WDT, 00h → WDT prescaler	1	$\overline{TO}$, $\overline{PD}$
IOST	**R**	Load IOST register	ACC → IOST register	1	-
RETURN		Return from subroutine	Top of Stack → PC	2	-
CLRA		Clear ACC	00h → ACC	1	Z
CLRR	**R**	Clear R	00h → R	1	Z
MOVAR	**R**	Move ACC to R	ACC → R	1	-
MOVR	**R, d**	Move R	R → dest	1	Z
DECR	**R, d**	Decrement R	R - 1 → dest	1	Z
DECRSZ	**R, d**	Decrement R, Skip if 0	R - 1 → dest, Skip if result = 0	1/2	-
INCR	**R, d**	Increment R	R + 1 → dest	1	Z
INCRSZ	**R, d**	Increment R, Skip if 0	R + 1 → dest, Skip if result = 0	1/2	-
ADDAR	**R, d**	Add ACC and R	R + ACC → dest	1	C, DC, Z
SUBAR	**R, d**	Subtract ACC from R	R - ACC → dest	1	C, DC, Z
ANDAR	**R, d**	AND ACC with R	ACC and R → dest	1	Z
IORAR	**R, d**	Inclusive OR ACC with R	ACC or R → dest	1	Z
XORAR	**R, d**	Exclusive OR ACC with R	R xor ACC → dest	1	Z
COMR	**R, d**	Complement R	$\overline{R}$ → dest	1	Z
RLR	**R, d**	Rotate left R through Carry	R<7> → C, R<6:0> → dest<7:1>, C → dest<0>	1	C
RRR	**R, d**	Rotate right R through Carry	C → dest<7>, R<7:1> → dest<6:0>, R<0> → C	1	C
SWAPR	**R, d**	Swap R	R<3:0> → dest<7:4>, R<7:4> → dest<3:0>	1	-
MOVIA	**I**	Move Immediate to ACC	I → ACC	1	-
ADDIA	**I**	Add ACC and Immediate	I + ACC → ACC	1	C, DC, Z
SUBIA	**I**	Subtract ACC from Immediate	I - ACC → ACC	1	C, DC, Z
ANDIA	**I**	AND Immediate with ACC	ACC and I → ACC	1	Z
IORIA	**I**	OR Immediate with ACC	ACC or I → ACC	1	Z
XORIA	**I**	Exclusive OR Immediate to ACC	ACC xor I → ACC	1	Z

RETIA	**I**	Return, place Immediate in ACC	I → ACC, Top of Stack → PC	2	-
CALL	**I**	Call subroutine	PC + 1 → Top of Stack, I → PC<8:0>	2	-
GOTO	**I**	Unconditional branch	I → PC<8:0>	2	-

Note: bit : Bit address within an 8-bit register R
R : Register address (00h to 3Fh)
I : Immediate data
ACC : Accumulator
d : Destination select;
=0 (store result in ACC)
=1 (store result in file register R)
dest : Destination
PC : Program Counter
WDT : Watchdog Timer Counter
$\overline{TO}$: Time-out bit
$\overline{PD}$: Power-down bit
C : Carry bit
DC : Digital carry bit
Z : Zero bit

ADDAR	**Add ACC and R**
Syntax:	ADDAR R, d
Operands:	$0 \le R \le 63$ $d \in [0,1]$
Operation:	ACC + R → dest
Status Affected:	C, DC, Z
Description:	Add the contents of the ACC register and register 'R'. If 'd' is 0 the result is stored in the ACC register. If 'd' is '1' the result is stored back in register 'R'.
Cycles:	1

ADDIA	**Add ACC and Immediate**
Syntax:	ADDIA I
Operands:	$0 \le I \le 255$
Operation:	ACC + I → ACC
Status Affected:	C, DC, Z
Description:	Add the contents of the ACC register with the 8-bit immediate 'I'. The result is placed in the ACC register.
Cycles:	1

ANDAR	**AND ACC and R**
Syntax:	ANDAR R, d
Operands:	$0 \le R \le 63$ $d \in [0,1]$
Operation:	ACC and R → dest
Status Affected:	Z
Description:	The contents of the ACC register are AND'ed with register 'R'. If 'd' is 0 the result is stored in the ACC register. If 'd' is '1' the result is stored back in register 'R'.
Cycles:	1

ANDIA	**AND Immediate with ACC**
Syntax:	ANDIA I
Operands:	$0 \le I \le 255$
Operation:	ACC AND I → ACC
Status Affected:	Z
Description:	The contents of the ACC register are AND'ed with the 8-bit immediate 'I'. The result is placed in the ACC register.
Cycles:	1

BCR	**Clear Bit in R**
Syntax:	BCF R, b
Operands:	$0 \le R \le 63$ $0 \le b \le 7$
Operation:	0 → R<b>
Status Affected:	None
Description:	Clear bit 'b' in register 'R'.
Cycles:	1

BSR	**Set Bit in R**
Syntax:	BSR R, b
Operands:	$0 \le R \le 63$ $0 \le b \le 7$
Operation:	1 → R<b>
Status Affected:	None
Description:	Set bit 'b' in register 'R'.
Cycles:	1

BTRSC	**Test Bit in R, Skip if Clear**
Syntax:	BTRSC R, b
Operands:	$0 \le R \le 63$ $0 \le b \le 7$
Operation:	Skip if R<b> = 0
Status Affected:	None
Description:	If bit 'b' in register 'R' is 0 then the next instruction is skipped. If bit 'b' is 0 then next instruction fetched during the current instruction execution is discarded, and a NOP is executed instead making this a 2-cycle instruction.
Cycles:	1/2

BTRSS	**Test Bit in R, Skip if Set**
Syntax:	BTRSS R, b
Operands:	$0 \le R \le 63$ $0 \le b \le 7$
Operation:	Skip if R<b> = 1
Status Affected:	None
Description:	If bit 'b' in register 'R' is '1' then the next instruction is skipped. If bit 'b' is '1', then the next instruction fetched during the current instruction execution, is discarded and a NOP is executed instead, making this a 2-cycle instruction.
Cycles:	1/2

CALL	**Subroutine Call**
Syntax:	CALL I
Operands:	$0 \le I \le 511$
Operation:	PC +1 → Top of Stack; I → PC<8:0>
Status Affected:	None
Description:	Subroutine call. First, return address (PC+1) is pushed onto the stack. The 9-bit immediate address is loaded into PC bits <8:0>. CALL is a two-cycle instruction.
Cycles:	2

CLRA	**Clear ACC**
Syntax:	CLRA
Operands:	None
Operation:	00h → ACC; 1 → Z
Status Affected:	Z
Description:	The ACC register is cleared. Zero bit (Z) is set.
Cycles:	1

CLRR	**Clear R**
Syntax:	CLRR R
Operands:	$0 \le R \le 63$
Operation:	00h → R; 1 → Z
Status Affected:	Z
Description:	The contents of register 'R' are cleared and the Z bit is set.
Cycles:	1

CLRWDT	**Clear Watchdog Timer**
Syntax:	CLRWDT
Operands:	None
Operation:	00h → WDT; 00h → WDT prescaler (if assigned); 1 → $\overline{TO}$; 1 → $\overline{PD}$
Status Affected:	$\overline{TO}$, $\overline{PD}$
Description:	The CLRWDT instruction resets the WDT. It also resets the prescaler, if the prescaler is assigned to the WDT and not Timer0. Status bits $\overline{TO}$ and $\overline{PD}$ are set.
Cycles:	1

COMR	**Complement R**
Syntax:	COMR R, d
Operands:	$0 \le R \le 63$ $d \in [0,1]$
Operation:	$\overline{R}$ → dest
Status Affected:	Z
Description:	The contents of register 'R' are complemented. If 'd' is 0 the result is stored in the ACC register. If 'd' is 1 the result is stored back in register 'R'.
Cycles:	1

DECR	**Decrement R**
Syntax:	DECR R, d
Operands:	$0 \le R \le 63$ $d \in [0,1]$
Operation:	R - 1 → dest
Status Affected:	Z
Description:	Decrement register 'R'. If 'd' is 0 the result is stored in the ACC register. If 'd' is 1 the result is stored back in register 'R'.
Cycles:	1

DECRSZ	**Decrement R, Skip if 0**
Syntax:	DECRSZ R, d
Operands:	$0 \le R \le 63$ $d \in [0,1]$
Operation:	R - 1 → dest; skip if result =0
Status Affected:	None
Description:	The contents of register 'R' are decremented. If 'd' is 0 the result is placed in the ACC register. If 'd' is 1 the result is placed back in register 'R'. If the result is 0, the next instruction, which is already fetched, is discarded and a NOP is executed instead making it a 2-cycle instruction.
Cycles:	1/2

GOTO	**Unconditional Branch**
Syntax:	GOTO I
Operands:	$0 \leq I \leq 511$
Operation:	I → PC<8:0>
Status Affected:	None
Description:	GOTO is an unconditional branch. The 9-bit immediate value is loaded into PC bits <8:0>. GOTO is a two-cycle instruction.
Cycles:	2

INCR	**Increment R**
Syntax:	INCR R, d
Operands:	$0 \leq R \leq 63$ $d \in [0,1]$
Operation:	R + 1 → dest
Status Affected:	Z
Description:	The contents of register 'R' are incremented. If 'd' is 0 the result is placed in the ACC register. If 'd' is 1 the result is placed back in register 'R'.
Cycles:	1

INCRSZ	**Increment R, Skip if 0**
Syntax:	INCRSZ R, d
Operands:	$0 \leq R \leq 63$ $d \in [0,1]$
Operation:	R + 1 → dest, skip if result = 0
Status Affected:	None
Description:	The contents of register 'R' are incremented. If 'd' is 0 the result is placed in the ACC register. If 'd' is the result is placed back in register 'R'. If the result is 0, then the next instruction, which is already fetched, is discarded and a NOP is executed instead making it a 2-cycle instruction.
Cycles:	1/2

IORAR	**OR ACC with R**
Syntax:	IORAR R, d
Operands:	$0 \leq R \leq 63$ $d \in [0,1]$
Operation:	ACC or R → dest
Status Affected:	Z
Description:	Inclusive OR the ACC register with register 'R'. If 'd' is 0 the result is placed in the ACC register. If 'd' is 1 the result is placed back in register 'R'.
Cycles:	1

IORIA	**OR Immediate with ACC**
Syntax:	IORIA I
Operands:	$0 \leq I \leq 255$
Operation:	ACC or I → ACC
Status Affected:	Z
Description:	The contents of the ACC register are OR'ed with the 8-bit immediate 'I'. The result is placed in the ACC register.
Cycles:	1

IOST	**Load IOST Register**
Syntax:	IOST R
Operands:	R = 5,6
Operation:	ACC → IOST register R
Status Affected:	None
Description:	IOST register 'R' (R = 5,6) is loaded with the contents of the ACC register.
Cycles:	1

MOVAR	**Move ACC to R**
Syntax:	MOVAR R
Operands:	$0 \leq R \leq 63$
Operation:	ACC → R
Status Affected:	None
Description:	Move data from the ACC register to register 'R'.
Cycles:	1

MOVIA	**Move Immediate to ACC**
Syntax:	MOVIA I
Operands:	$0 \leq I \leq 255$
Operation:	I → ACC
Status Affected:	None
Description:	The 8-bit immediate 'I' is loaded into the ACC register. The don't cares will assemble as 0s.
Cycles:	1

MOVR	**Move R**
Syntax:	MOVR R, d
Operands:	$0 \leq R \leq 63$ $d \in [0,1]$
Operation:	R → dest
Status Affected:	Z
Description:	The contents of register 'R' is moved to destination 'd'. If 'd' is 0, destination is the ACC register. If 'd' is 1, the destination is file register 'R'. 'd' is 1 is useful to test a file register since status flag Z is affected.
Cycles:	1

NOP	**No Operation**
Syntax:	NOP
Operands:	None
Operation:	No operation
Status Affected:	None
Description:	No operation.
Cycles:	1

OPTION	**Load OPTION Register**
Syntax:	OPTION
Operands:	None
Operation:	ACC → OPTION
Status Affected:	None
Description:	The content of the ACC register is loaded into the OPTION register.
Cycles:	1

RETIA	**Return with Immediate in ACC**
Syntax:	RETIA I
Operands:	$0 \leq I \leq 255$
Operation:	I → ACC; Top of Stack → PC
Status Affected:	None
Description:	The ACC register is loaded with the 8-bit immediate 'I'. The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction.
Cycles:	2

RETURN	**Return from Subroutine**
Syntax:	RETURN
Operands:	None
Operation:	Top of Stack → PC
Status Affected:	None
Description:	The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction.
Cycles:	2

RLR	**Rotate Left R through Carry**
Syntax:	RLR R, d
Operands:	$0 \leq R \leq 63$ $d \in [0,1]$
Operation:	R<7> → C; R<6:0> → dest<7:1>; C → dest<0>
Status Affected:	C
Description:	The contents of register 'R' are rotated one bit to the left through the Carry Flag. If 'd' is 0 the result is placed in the ACC register. If 'd' is 1 the result is stored back in register 'R'.
Cycles:	1

RRR	**Rotate Right R through Carry**
Syntax:	RRR R, d
Operands:	$0 \leq R \leq 63$ $d \in [0,1]$
Operation:	C → dest<7>; R<7:1> → dest<6:0>; R<0> → C
Status Affected:	C
Description:	The contents of register 'R' are rotated one bit to the right through the Carry Flag. If 'd' is 0 the result is placed in the ACC register. If 'd' is 1 the result is placed back in register 'R'.
Cycles:	1

SLEEP	**Enter SLEEP Mode**
Syntax:	SLEEP
Operands:	None
Operation:	00h → WDT; 00h → WDT prescaler; 1 → $\overline{TO}$; 0 → $\overline{PD}$
Status Affected:	$\overline{TO}$, $\overline{PD}$
Description:	Time-out status bit ($\overline{TO}$) is set. The power-down status bit ($\overline{PD}$) is cleared. The WDT and its prescaler are cleared. The processor is put into SLEEP mode.
Cycles:	1

SUBAR	**Subtract ACC from R**
Syntax:	SUBAR R, d
Operands:	$0 \le R \le 63$ $d \in [0,1]$
Operation:	R - ACC → dest
Status Affected:	C, DC, Z
Description:	Subtract (2's complement method) the ACC register from register 'R'. If 'd' is 0 the result is stored in the ACC register. If 'd' is 1 the result is stored back in register 'R'.
Cycles:	1

SUBIA	**Subtract ACC from Immediate**
Syntax:	SUBIA I
Operands:	$0 \le I \le 255$
Operation:	I - ACC → ACC
Status Affected:	C, DC, Z
Description:	Subtract (2's complement method) the ACC register from the 8-bit immediate 'I'. The result is placed in the ACC register.
Cycles:	1

SWAPR	**Swap nibbles in R**
Syntax:	SWAPR R, d
Operands:	$0 \le R \le 63$ $d \in [0,1]$
Operation:	R<3:0> → dest<7:4>; R<7:4> → dest<3:0>
Status Affected:	None
Description:	The upper and lower nibbles of register 'R' are exchanged. If 'd' is 0 the result is placed in ACC register. If 'd' is 1 the result in placed in register 'R'.
Cycles:	1

XORAR	**Exclusive OR ACC with R**
Syntax:	XORAR R, d
Operands:	$0 \le R \le 63$ $d \in [0,1]$
Operation:	ACC xor R → dest
Status Affected:	Z
Description:	Exclusive OR the contents of the ACC register with register 'R'. If 'd' is 0 the result is stored in the ACC register. If 'd' is 1 the result is stored back in register 'R'.
Cycles:	1

XORIA	**Exclusive OR Immediate with ACC**
Syntax:	XORIA I
Operands:	$0 \leq I \leq 255$
Operation:	ACC xor I → ACC
Status Affected:	Z
Description:	The contents of the ACC register are XOR'ed with the 8-bit immediate 'I'. The result is placed in the ACC register.
Cycles:	1

3.0 ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	0℃ to +70℃
Store Temperature	-65℃ to +150℃
DC Supply Voltage (Vdd)	0V to +6.0V
Input Voltage with respect to Ground (Vss)	-0.3V to (Vdd + 0.3)V

4.0 OPERATING CONDITIONS

DC Supply Voltage	+2.3V to +5.5V
Operating Temperature	0℃ to +70℃

5.0 ELECTRICAL CHARACTERISTICS

6.1 ELECTRICAL CHARACTERISTICS of FM8A23E

Under Operating Conditions (Vdd = 3V, temperature = 25℃), and WDT & LVDT are disabled

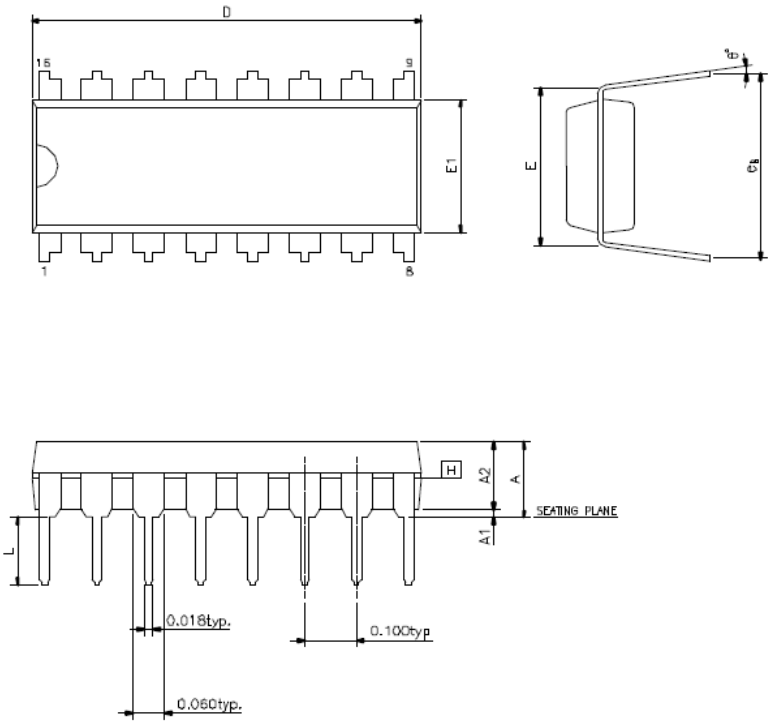
Sym	Description	Conditions			Min.	Typ.	Max.	Unit
F_{XT}	X'tal oscillation range	XT mode				455		KHz
F_{ERC}	RC oscillation range	ERC mode			DC		4	MHz
V_{IH}	Input high voltage				1.5			V
V_{IL}	Input low voltage						0.6	V
V_{OH}	Output high voltage	IROUT, I_{OH}=-2mA			2.7			V
		Other pins, I_{OH}=-25uA			2.7			V
V_{OL}	Output low voltage	IROUT, IRPOL = 0, I_{OL}=5mA					0.3	V
		IROUT, IRPOL = 1, I_{OL}=200mA					0.3	V
		Other pins, I_{OL}=700uA					0.3	V
I_{PH}	Pull-high current	Input pin at Vss				-100		uA
I_{WDT}	WDT current					1	3	uA
T_{WDT}	WDT period					20		mS
I_{LVDT}	LVDT current					2	3	uA
I_{SB}	Power down current	Sleep mode, WDT enable				2.1		uA
		Sleep mode, WDT disable				1.1		
I_{DD}	Operating current	XT mode						uA
		455KHz						
I_{DD}	Operating current	ERC mode						mA
		C=3P	R=1Kohm	F=8.306MHz				
			R=3.3Kohm	F=7.29MHz				
			R=10Kohm	F=4.81MHz				
			R=100Kohm	F=904KHz				
			R=300Kohm	F=338KHz				
		C=20P	R=1Kohm	F=7.08MHz				
			R=3.3Kohm	F=5.07MHz				
			R=10Kohm	F=2.68MHz				
			R=100Kohm	F=362KHz				
			R=300Kohm	F=123KHz				
		C=100P	R=1Kohm	F=4.11MHz				
			R=3.3Kohm	F=2.03MHz				
			R=10Kohm	F=810KHz				
			R=100Kohm	F=91KHz				
			R=300Kohm	F=30KHz				

6.2 ELECTRICAL CHARACTERISTICS of FM8A23

To be defined

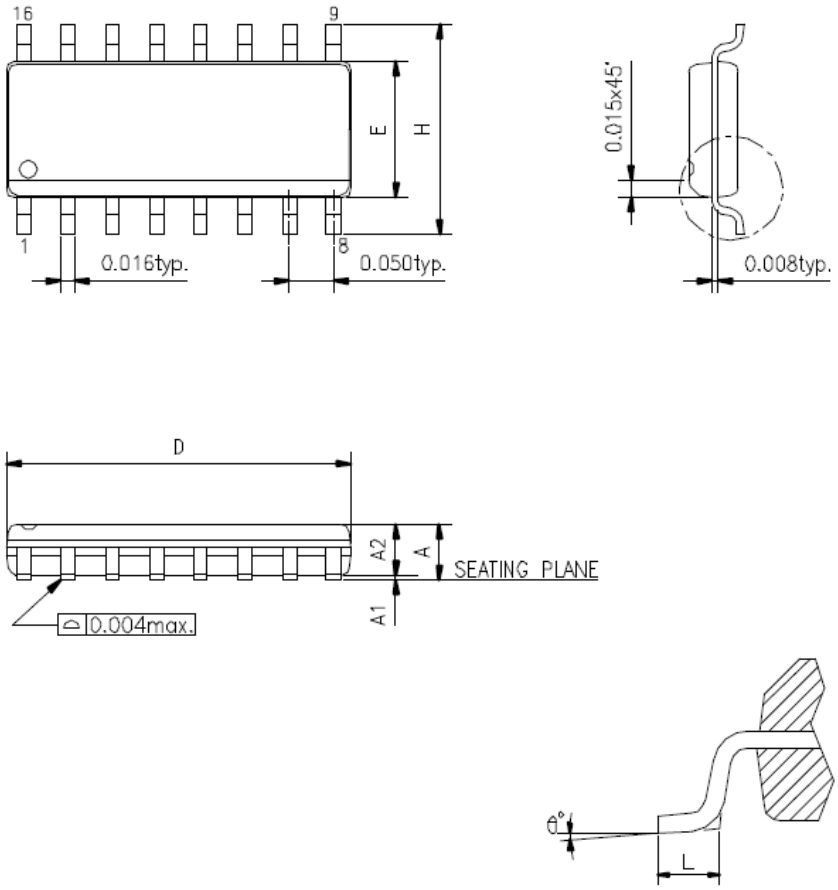
7.0 PACKAGE DIMENSION

7.1 16-PIN PDIP 300mil



Symbols	Dimension In Inches		
	Min	Nom	Max
A	-	-	0.210
A1	0.015	-	-
A2	0.125	0.130	0.135
D	0.735	0.755	0.775
E	0.300 BSC		
E1	0.245	0.250	0.255
L	0.115	0.130	0.150
e_B	0.335	0.355	0.375
θ°	0°	7°	15°

7.2 16-PIN SOP 150mil



Symbols	Dimension In Inches		
	Min	Nom	Max
A	0.053	-	0.069
A1	0.004	-	0.010
A2	0.049	-	0.065
D	0.386	-	0.394
E	0.150	-	0.157
H	0.228	-	0.244
L	0.016	-	0.050
θ°	0°	-	8°

8.0 ORDERING INFORMATION

OTP Type MCU	Package Type	Pin Count	Package Size
FM8A23EP	PDIP	16	300 mil
FM8A23ED	SOP	16	150 mil

Mask Type MCU	Package Type	Pin Count	Package Size
FM8A23P	PDIP	16	300 mil
FM8A23D	SOP	16	150 mil