FEELING TECHNOLOGY

FM8PE53M

OTP-Based 8-Bit Microcontroller

Devices Included in this Data Sheet:

- FM8PE53M: OTP device

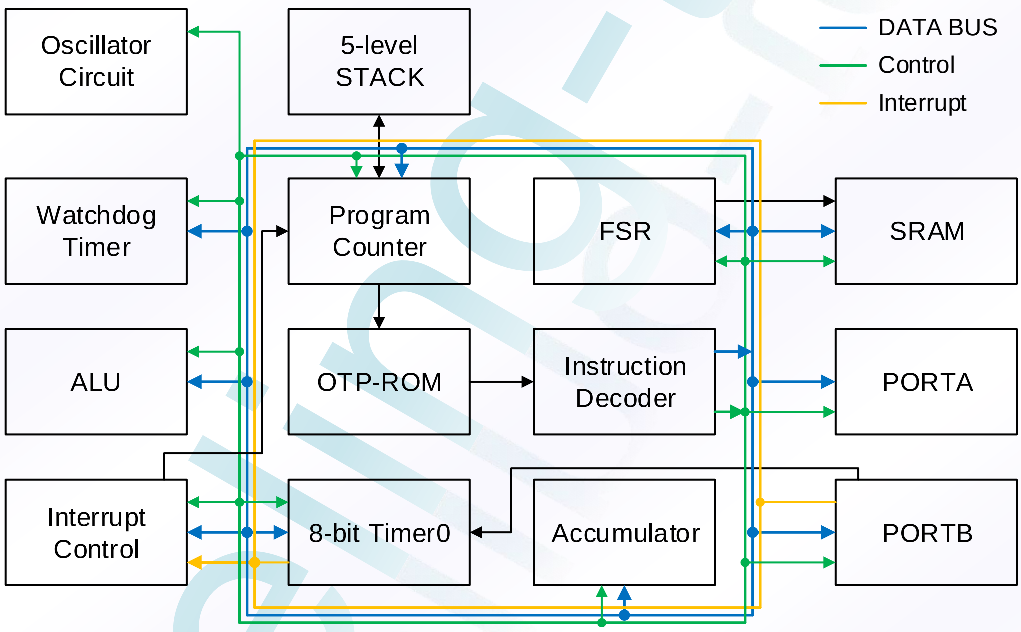
FEATURES

- 1K Word on chip OTP
- 49x8 bits on chip general purpose registers (SRAM)
- 8-bit wide data path
- 5-level deep hardware stack
- Only 42 single word instructions
- All instructions are single cycle except for program branches which are two-cycle
- All OTP area GOTO instruction
- All OTP area subroutine CALL instruction
- Direct, indirect addressing modes for data accessing
- 8-bit real time clock/counter (Timer0) with 8-bit programmable pre-scaler
- Internal Power-on Reset (POR)
- Built-in Low Voltage Detector (LVD) for Brown-out Reset (BOR)
- Power-up Reset Timer (PWRT) and Oscillator Start-up Timer(OST)
- On chip Watchdog Timer (WDT) with internal oscillator for reliable operation and soft-ware watch-dog enable/disable control
- Two I/O ports IOA and IOB with independent direction control
- Soft-ware I/O pull-high/pull-down or open-drain control
- One internal interrupt source: Timer0 overflow; Two external interrupt source: INT pin, Port B input change
- Wake-up from SLEEP by INT pin or Port B input change
- Power saving SLEEP mode
- Built-in $8M_{HZ}$, $4M_{HZ}$, $1M_{HZ}$, and $455K_{HZ}$ internal RC oscillator
- Programmable Code Protection
- Selectable oscillator options:
  - ERC: External Resistor/Capacitor Oscillator
  - HF: High Frequency Crystal/Resonator Oscillator
  - XT: Crystal/Resonator Oscillator
  - LF: Low Frequency Crystal Oscillator
  - IRC: Internal Resistor/Capacitor Oscillator
  - ERIC: External Resistor/Internal Capacitor Oscillator
- Operating voltage range: 2.0V to 5.5V

GENERAL DESCRIPTION

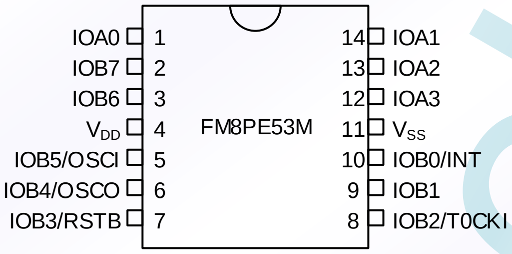
The FM8PE53M is a low-cost, high speed, high noise immunity, OTP-based 8-bit CMOS microcontrollers. It employs a RISC architecture with only 42 instructions. All instructions are single cycle except for program branches which take two cycles. The easy to use and easy to remember instruction set reduces development time significantly.
The FM8PE53M consists of Power-on Reset (POR), Brown-out Reset (BOR), Power-up Reset Timer (PWRT), Oscillator Start-up Timer(OST), Watchdog Timer, OTP, SRAM, tristate I/O port, I/O pull-high/open-drain/pull-down control, Power saving SLEEP mode, real time programmable clock/counter, Interrupt, Wake-up from SLEEP mode, and Code Protection for OTP products. There are three oscillator configurations to choose from, including the external clock input, external resistor RC oscillator and internal RC oscillator.
The FM8PE53M address 1K of program memory.
The FM8PE53M can directly or indirectly address its register files and data memory. All special function registers including the program counter are mapped in the data memory.

BLOCK DIAGRAM



PIN CONNECTION

PDIP, SOP



PIN DESCRIPTIONS

Name	I/O	Description
IOA0 ~ IOA3	I/O	• IOA0 ~ IOA3 as bi-direction I/O pin. • Software controlled pull-down.
IOB0/INT	I/O	• Bi-direction I/O pin with system wake-up function. • Software controlled pull-high/open-drain/pull-down. • External interrupt input.
IOB1	I/O	• Bi-direction I/O pin with system wake-up function. • Software controlled pull-high/open-drain/pull-down.
IOB2/T0CKI	I/O	• Bi-direction I/O pin with system wake-up function. • Software controlled pull-high/open-drain/pull-down. • External clock input to Timer0.
IOB3/RSTB	I/O	• Input pin or open-drain output pin with system wake-up function. • System clear (RESET) input. Active low RESET to the device. Weak pull-high always on if configured as RSTB. • **Voltage on this pin must not exceed V_{DD},** See IOB3 diagram for detail description.
IOB4/OSCO	I/O	• Bi-direction I/O pin with system wake-up function (RCOUT optional in IRC/ERIC, ERC mode). • Software controlled pull-high/open-drain. • Oscillator crystal output (HF, XT, LF mode). • Outputs with the instruction cycle rate (RCOUT optional in IRC/ERIC, ERC mode).
IOB5/OSCI	I/O	• Bi-direction I/O pin with system wake-up function (IRC mode). • Software controlled pull-high/open-drain. • Oscillator crystal input (HF, XT, LF mode). • External clock source input (ERIC, ERC mode).
IOB6 ~ IOB7	I/O	• Bi-direction I/O pin with system wake-up function. • Software controlled pull-high/open-drain.
V_{DD}	-	Positive supply.
V_{SS}	-	Ground.

Legend: I=input, O=output, I/O=input/output

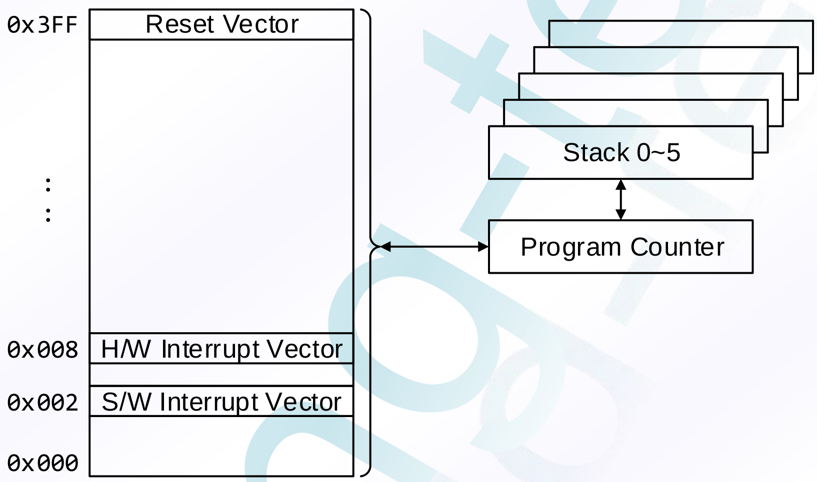
1.0 MEMORY ORGANIZATION

FM8PE53M memory is organized into program memory and data memory.

1.1 Program Memory Organization

The FM8PE53M has a 10-bit Program Counter capable of addressing a 1K program memory space.
The RESET vector for the FM8PE53M is at 0x3FF.
The H/W interrupt vector is at 0x008. And the S/W interrupt vector is at 0x002.
FM8PE53M supports all OTP area CALL/GOTO instructions without page.

Figure 1.1: Program Memory Map and STACK



1.2 Data Memory Organization

Data memory is composed of Special Function Registers and General Purpose Registers.
The General-Purpose Registers are accessed either directly or indirectly through the FSR register.
The Special Function Registers are registers used by the CPU and peripheral functions to control the operation of the device.

Table 1.1: Registers File Map for FM8PE53M

Address	Description
0x00	INDF
0x01	TMR0
0x02	PCL
0x03	STATUS
0x04	FSR
0x05	PORTA
0x06	PORTB
0x07	General Purpose Register
0x08	PCON
0x09	WUCON
0x0A	PCHBUF
0x0B	PDCON
0x0C	ODCON
0x0D	PHCON
0x0E	INTEN
0x0F	INTFLAG
0x10 ~ 0x3F	General Purpose Registers

N/A	OPTION
0x05	IOSTA
0x06	IOSTB

Table 1.2: The Registers Controlled by OPTION or IOST Instructions

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
N/A (w)	OPTION	*	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
0x05 (w)	IOSTA	Port A I/O Control Register							
0x06 (w)	IOSTB	Port B I/O Control Register							

Table 1.3: Operational Registers Map

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x00 (r/w)	INDF	Uses contents of FSR to address data memory (not a physical register)							
0x01 (r/w)	TMR0	8-bit real-time clock/counter							
0x02 (r/w)	PCL	Low order 8 bits of PC							
0x03 (r/w)	STATUS	RST			$\overline{TO}$	$\overline{PD}$	Z	DC	C
0x04 (r/w)	FSR	*	*	Indirect data memory address pointer					
0x05 (r/w)	PORTA					IOA3	IOA2	IOA1	IOA0
0x06 (r/w)	PORTB	IOB7	IOB6	IOB5	IOB4	IOB3	IOB2	IOB1	IOB0
0x07 (r/w)	SRAM	General Purpose Register							
0x08 (r/w)	PCON	WDTE	EIS	LVDTE	*	*	*	*	*
0x09 (r/w)	WUCON	WUB7	WUB6	WUB5	WUB4	WUB3	WUB2	WUB1	WUB0
0x0A (r/w)	PCHBUF	-	-	-	-	-	-	2 MSBs Buffer of PC	
0x0B (r/w)	PDCON		/PDB2	/PDB1	/PDB0	/PDA3	/PDA2	/PDA1	/PDA0
0x0C (r/w)	ODCON	ODB7	ODB6	ODB5	ODB4		ODB2	ODB1	ODB0
0x0D (r/w)	PHCON	/PHB7	/PHB6	/PHB5	/PHB4		/PHB2	/PHB1	/PHB0
0x0E (r/w)	INTEN	GIE	*	*	*	*	INTIE	PBIE	T0IE
0x0F (r/w)	INTFLAG	-	-	-	-	-	INTIF	PBIF	T0IF

Legend: - = unimplemented, read as ‘0’, * = unimplemented, read as ‘1’.

2.0 FUNCTIONAL DESCRIPTIONS

2.1 Operational Registers

2.1.1 INDF (Indirect Addressing Register)

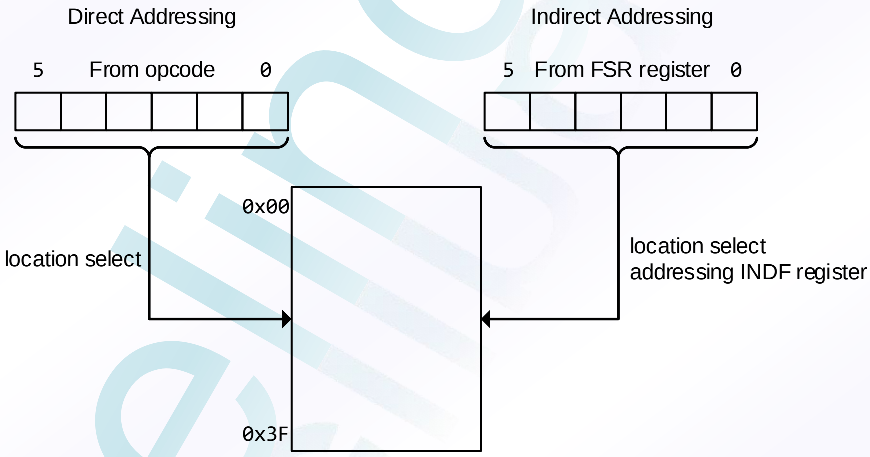
Read/Write-POR		R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x00	INDF	Uses contents of FSR to address data memory (not a physical register)							

Legend: x = unknown, more bits' default state, please refer to Table 2.2.

The INDF Register is not a physical register. Any instruction accessing the INDF register can actually access the register pointed by FSR Register. Reading the INDF register itself indirectly (FSR="0x00") will read 0x00. Writing to the INDF register indirectly results in a no-operation (although status bits may be affected).
The bits 5-0 of FSR register are used to select up to 64 registers (address: 0x00 ~ 0x3F).

Example 2.1: INDIRECT ADDRESSING
- Register file 0x38 contains the value 0x10
- Register file 0x39 contains the value 0x0A
- Load the value 0x38 into the FSR Register
- A read of the INDF Register will return the value of 0x10
- Increment the value of the FSR Register by one (@FSR=0x39)
- A read of the INDF register now will return the value of 0x0A.

Figure 2.1: Direct/Indirect Addressing



2.1.2 TMR0 (Time Clock/Counter register)

Read/Write-POR		R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x01	TMR0	8-bit real-time clock/counter							

Note: more bits' default state, please refer to Table 2.2.

The Timer0 is a 8-bit timer/counter. The clock source of Timer0 can come from the instruction cycle clock or by an external clock source (T0CKI pin) defined by T0CS bit (OPTION<5>). If T0CKI pin is selected, the Timer0 is increased by T0CKI signal rising/falling edge (selected by T0SE bit (OPTION<4>)).
The pre-scaler is assigned to Timer0 by clearing the PSA bit (OPTION<3>). In this case, the pre-scaler will be cleared when TMR0 register is written with a value.

2.1.3 PCL (Low Bytes of Program Counter) & Stack

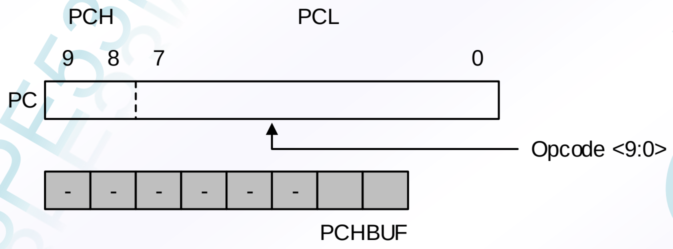
Read/Write-POR		R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x02	PCL	Low order 8 bits of PC							

Note: more bits' default state, please refer to Table 2.2.

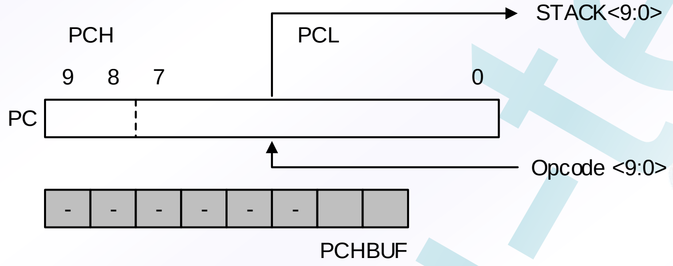
FM8PE53M device has a 10-bit wide Program Counter (PC) and five-level deep 10-bit hardware push/pop stack. The low byte of PC is called the PCL register. This register is readable and writable. The high byte of PC is called the PCH register. This register contains the PC<9:8> bits and is not directly readable or writable. All updates to the PCH register go through the PCHBUF register. As a program instruction is executed, the Program Counter will contain the address of the next program instruction to be executed. The PC value is increased by one, every instruction cycle, unless an instruction changes the PC.
For a GOTO instruction, the PC<9:0> is provided by the GOTO instruction word. The PCL register is mapped to PC<7:0>, and the PCHBUF register is not updated.
For a CALL instruction, the PC<9:0> is provided by the CALL instruction word. The next PC will be loaded (PUSHed) onto the top of STACK. The PCL register is mapped to PC<7:0>, and the PCHBUF register is not updated.
For a RETIA, RETFIE, or RETURN instruction, the PC are updated (POPed) from the top of STACK. The PCL register is mapped to PC<7:0>, and the PCHBUF register is not updated.
For any instruction where the PCL is the destination, the PC<7:0> is provided by the instruction word or ALU result. However, the PC<9:8> will come from the PCHBUF<1:0> bits (PCHBUF → PCH).
PCHBUF register is never updated with the contents of PCH.

Figure 2.2: Loading of PC in Different Situations

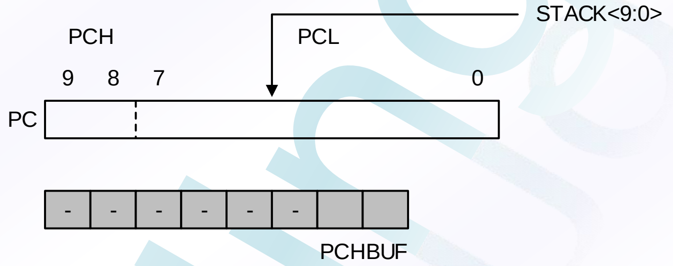
Situation 1: **GOTO** Instruction



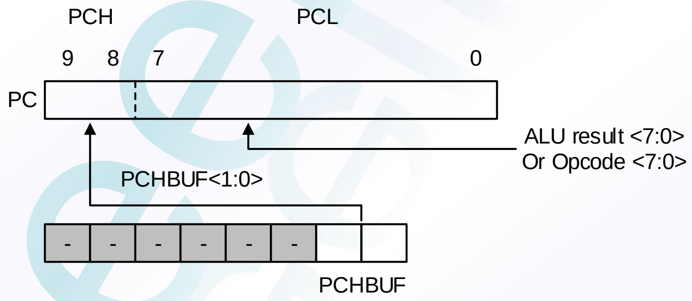
Situation 2: **CALL** Instruction



Situation 3: **RETIA**, **RETFIE**, or **RETURN** Instruction



Situation 4: Instruction with PCL as destination



Note: PCHBUF is used only for instruction with PCL as destination for FM8PE53M.

2.1.4 STATUS (Status Register)

Read/Write-POR		R/W-0	R/W-0	R/W-0	R-#	R-#	R/W-x	R/W-x	R/W-x
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x03	STATUS	RST			$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C

Legend: x = unknown, # refer Table 2.3 for detail description, more bits' default state, please refer to Table 2.2.

This register contains the arithmetic status of the ALU, the RESET status.
If the STATUS Register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits are not writable. Therefore, the result of an instruction with the STATUS Register as destination may be different than intended. For example, CLRR STATUS will clear the upper three bits and set the Z bit. This leaves the STATUS Register as 000u u1uu (where u = unchanged).

C: Carry/borrow bit.
ADDAR, ADDIA, ADCAR
= 0, No Carry occurred.
= 1, Carry occurred.
SUBAR, SUBIA, SBCAR
= 0, Borrow occurred.
= 1, No borrow occurred.
Note: A subtraction is executed by adding the two's complement of the second operand. For rotate (RRR, RLR) instructions, this bit is loaded with either the high or low order bit of the source register.

DC: Half carry/half borrow bit
ADDAR, ADDIA, ADCAR
= 0, No Carry from the 4th low order bit of the result occurred.
= 1, Carry from the 4th low order bit of the result occurred.
SUBAR, SUBIA, SBCAR
= 0, Borrow from the 4th low order bit of the result occurred.
= 1, No Borrow from the 4th low order bit of the result occurred.

Z: Zero bit.
= 0, The result of a logic operation is not zero.
= 1, The result of a logic operation is zero.

$\overline{\text{PD}}$: Power down flag bit.
= 0, by the SLEEP instruction.
= 1, after power-up or by the CLRWDT instruction.

$\overline{\text{TO}}$: Time overflow flag bit.
= 0, a watch-dog time overflow occurred.
= 1, after power-up or by the CLRWDT or SLEEP instruction.

Bit6:Bit5: General purpose read/write bit.

RST: Bit for wake-up type.
= 0, Wake-up from other reset types.
= 1, Wake-up from SLEEP on Port B input change.

2.1.5 FSR (Indirect Data Memory Address Pointer)

Read/Write-POR		*	*	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x04	FSR	*	*	Indirect data memory address pointer					

Legend: * = unimplemented, read as '1', more bits' default state, please refer to Table 2.2.

Bit5:Bit0: Select registers address in the indirect addressing mode. See 2.1.1 for detail description.

2.1.6 PORTA, PORTB (Port Data Registers)

Read/Write-POR		R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x05	PORTA					IOA3	IOA2	IOA1	IOA0

Read/Write-POR		R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x06	PORTB	IOB7	IOB6	IOB5	IOB4	IOB3	IOB2	IOB1	IOB0

Note: more bits' default state, please refer to Table 2.2.

Reading the port (PORTA, PORTB register) reads the status of the pins independent of the pin's input/output modes. Writing to these ports will write to the port data latch.
PORTA is a 4-bit port data Register. Only the low order 4 bits are used (PORTA<3:0>). Bits 7-4 are general purpose read/write bits.

IOA3:IOA0: PORTA I/O pin.
= 0, Port pin is low level.
= 1, Port pin is high level.

IOB7:IOB0: PORTB I/O pin.
= 0, Port pin is low level.
= 1, Port pin is high level.
Note: IOB3 is open-drain output only if IOSTB3 = 0. See 2.1.17 for detail description.

2.1.7 PCON (Power Control Register)

Read/Write-POR		R/W-1	R/W-0	R/W-1	*	*	*	*	*
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x08	PCON	WDTE	EIS	LVDTE	*	*	*	*	*

Legend: * = unimplemented, read as '1', more bits' default state, please refer to Table 2.2.

LVDTE: LVDT (low voltage detector) enable bit.
= 0, Disable LVDT.
= 1, Enable LVDT.

EIS: Define the function of IOB0/INT pin.
= 0, IOB0 (bi-directional I/O pin) is selected. The path of INT is masked.
= 1, INT (external interrupt pin) is selected. In this case, the I/O control bit of IOB0 must be set to "1". The path of Port B input change of IOB0 pin is masked by hardware, the status of INT pin can also be read by way of reading PORTB.

WDTE: WDT (watch-dog timer) enable bit.
= 0, Disable WDT.
= 1, Enable WDT.

2.1.8 WUCON (Port B Input Change Interrupt/Wake-up Control Register)

Read/Write-POR		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x09	WUCON	WUB7	WUB6	WUB5	WUB4	WUB3	WUB2	WUB1	WUB0

Note: more bits' default state, please refer to Table 2.2.

WUB0: = 0, Disable the input change interrupt/wake-up function of IOB0 pin.
= 1, Enable the input change interrupt/wake-up function of IOB0 pin.

WUB1: = 0, Disable the input change interrupt/wake-up function of IOB1 pin.
= 1, Enable the input change interrupt/wake-up function of IOB1 pin.

WUB2: = 0, Disable the input change interrupt/wake-up function of IOB2 pin.
= 1, Enable the input change interrupt/wake-up function of IOB2 pin.

WUB3: = 0, Disable the input change interrupt/wake-up function of IOB3 pin.
= 1, Enable the input change interrupt/wake-up function of IOB3 pin.

WUB4: = 0, Disable the input change interrupt/wake-up function of IOB4 pin.
= 1, Enable the input change interrupt/wake-up function of IOB4 pin.

WUB5: = 0, Disable the input change interrupt/wake-up function of IOB5 pin.
= 1, Enable the input change interrupt/wake-up function of IOB5 pin.

WUB6: = 0, Disable the input change interrupt/wake-up function of IOB6 pin.
= 1, Enable the input change interrupt/wake-up function of IOB6 pin.

WUB7: = 0, Disable the input change interrupt/wake-up function of IOB7 pin.
= 1, Enable the input change interrupt/wake-up function of IOB7 pin.

2.1.9 PCHBUF (High Byte Buffer of Program Counter)

Read/Write-POR		-	-	-	-	-	-	R/W-1	R/W-1
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x0A	PCHBUF	-	-	-	-	-	-	2 MSBs Buffer of PC	

Legend: - = unimplemented, read as '0', more bits' default state, please refer to Table 2.2.

Bit1:Bit0: See 2.1.3 for detail description.

2.1.10 PDCON (Pull-down Control Register)

Read/Write-POR		R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x0B	PDCON		/PDB2	/PDB1	/PDB0	/PDA3	/PDA2	/PDA1	/PDA0

Note: more bits' default state, please refer to Table 2.2.

/PDA0: = 0, Enable the internal pull-down of IOA0 pin.
= 1, Disable the internal pull-down of IOA0 pin.

/PDA1: = 0, Enable the internal pull-down of IOA1 pin.
= 1, Disable the internal pull-down of IOA1 pin.

/PDA2: = 0, Enable the internal pull-down of IOA2 pin.
= 1, Disable the internal pull-down of IOA2 pin.

/PDA3: = 0, Enable the internal pull-down of IOA3 pin.
= 1, Disable the internal pull-down of IOA3 pin.

/PDB0: = 0, Enable the internal pull-down of IOB0 pin.
= 1, Disable the internal pull-down of IOB0 pin.

/PDB1: = 0, Enable the internal pull-down of IOB1 pin.
= 1, Disable the internal pull-down of IOB1 pin.

/PDB2: = 0, Enable the internal pull-down of IOB2 pin.
= 1, Disable the internal pull-down of IOB2 pin.

Bit7: General purpose read/write bit.

2.1.11 ODCON (Open-drain Control Register)

Read/Write-POR		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x0C	ODCON	ODB7	ODB6	ODB5	ODB4		ODB2	ODB1	ODB0

Note: more bits' default state, please refer to Table 2.2.

ODB0: = 0, Disable the internal open-drain of IOB0 pin.
= 1, Enable the internal open-drain of IOB0 pin.

ODB1: = 0, Disable the internal open-drain of IOB1 pin.
= 1, Enable the internal open-drain of IOB1 pin.

ODB2: = 0, Disable the internal open-drain of IOB2 pin.
= 1, Enable the internal open-drain of IOB2 pin.

Bit3: General purpose read/write bit.

ODB4: = 0, Disable the internal open-drain of IOB4 pin.
= 1, Enable the internal open-drain of IOB4 pin.

ODB5: = 0, Disable the internal open-drain of IOB5 pin.
= 1, Enable the internal open-drain of IOB5 pin.

ODB6: = 0, Disable the internal open-drain of IOB6 pin.
= 1, Enable the internal open-drain of IOB6 pin.

ODB7: = 0, Disable the internal open-drain of IOB7 pin.
= 1, Enable the internal open-drain of IOB7 pin.

2.1.12 PHCON (Pull-high Control Register)

Read/Write-POR		R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x0D	PHCON	/PHB7	/PHB6	/PHB5	/PHB4		/PHB2	/PHB1	/PHB0

Note: more bits' default state, please refer to Table 2.2.

/PHB0: = 0, Enable the internal pull-high of IOB0 pin.
= 1, Disable the internal pull-high of IOB0 pin.

/PHB1: = 0, Enable the internal pull-high of IOB1 pin.
= 1, Disable the internal pull-high of IOB1 pin.

/PHB2: = 0, Enable the internal pull-high of IOB2 pin.
= 1, Disable the internal pull-high of IOB2 pin.

Bit3: General purpose read/write bit.

/PHB4: = 0, Enable the internal pull-high of IOB4 pin.
= 1, Disable the internal pull-high of IOB4 pin.

/PHB5: = 0, Enable the internal pull-high of IOB5 pin.
= 1, Disable the internal pull-high of IOB5 pin.

/PHB6: = 0, Enable the internal pull-high of IOB6 pin.
= 1, Disable the internal pull-high of IOB6 pin.

/PHB7: = 0, Enable the internal pull-high of IOB7 pin.
= 1, Disable the internal pull-high of IOB7 pin.

2.1.13 INTEN (Interrupt Mask Register)

Read/Write-POR		R/W-0	*	*	*	*	R/W-0	R/W-0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x0E	INTEN	GIE	*	*	*	*	INTIE	PBIE	T0IE

Legend: * = unimplemented, read as '1', more bits' default state, please refer to Table 2.2.

T0IE: Timer0 overflow interrupt enable bit.
= 0, Disable the Timer0 overflow interrupt.
= 1, Enable the Timer0 overflow interrupt.

PBIE: Port B input change interrupt enable bit.
= 0, Disable the Port B input change interrupt.
= 1, Enable the Port B input change interrupt.

INTIE: External INT pin interrupt enable bit.
= 0, Disable the External INT pin interrupt.
= 1, Enable the External INT pin interrupt.

GIE: Global interrupt enable bit.
= 0, Disable all interrupts. For wake-up from SLEEP mode through an interrupt event, the device will continue execution at the instruction after the SLEEP instruction.
= 1, Enable all un-masked interrupts. For wake-up from SLEEP mode through an interrupt event, the device will branch to the interrupt address (0x008).
Note: When an interrupt event occurs with the GIE bit and its corresponding interrupt enable bit are all set, the GIE bit will be cleared by hardware to disable any further interrupts. The RETFIE instruction will exit the interrupt routine and set the GIE bit to re-enable interrupt.

2.1.14 INTFLAG (Interrupt Status Register)

Read/Write-POR		-	-	-	-	-	R/W-0	R/W-0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x0F	INTFLAG	-	-	-	-	-	INTIF	PBIF	T0IF

Legend: - = unimplemented, read as '0', more bits' default state, please refer to Table 2.2.

T0IF: Timer0 overflow interrupt flag. Set when Timer0 overflows, reset by software.

PBIF: Port B input change interrupt flag. Set when Port B input changes, reset by software.

INTIF: External INT pin interrupt flag. Set by rising/falling (selected by INTEDG bit (OPTION<6>)) edge on INT pin, reset by software.

2.1.15 ACC (Accumulator)

Read/Write-POR		R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
N/A	ACC	Accumulator							

Legend: x = unknown, more bits' default state, please refer to Table 2.2.

Accumulator is an internal data transfer, or instruction operand holding. It cannot be addressed.

2.1.16 OPTION Register

Read/Write-POR		W-1	W-0	W-1	W-1	W-1	W-1	W-1	W-1
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
N/A	OPTION	*	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0

Accessed by OPTION instruction.
Legend: * = unimplemented, more bits' default state, please refer to Table 2.2.

By executing the OPTION instruction, the contents of the ACC Register will be transferred to the OPTION Register. The OPTION Register is a 7-bit wide, write-only register which contains various control bits to configure the Timer0/WDT pre-scaler, Timer0, and the external INT interrupt.
The OPTION Register are "write-only" and are set all "1"s except INTEDG bit.

PS2:PS0: Pre-scaler rate selects bits.

PS2:PS0			Timer0 Rate	WDT Rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

PSA: Pre-scaler assign bit.
= 0, TMR0 (Timer0).
= 1, WDT (watch-dog timer).

T0SE: TMR0 source edge select bit.
= 0, Rising edge on T0CKI pin.
= 1, Falling edge on T0CKI pin.

T0CS: TMR0 clock source select bit.
= 0, internal instruction clock cycle.
= 1, External T0CKI pin. Pin IOB2/T0CKI is forced to be an input even if IOST IOB2 = "0".

INTEDG: Interrupt edge select bit.
= 0, interrupt on falling edge of INT pin.
= 1, interrupt on rising edge of INT pin.

2.1.17 IOSTA, IOSTB (Port I/O Control Registers)

Read/Write-POR		-	-	-	-	W-1	W-1	W-1	W-1
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x05	IOSTA	-	-	-	-	IOSTA3	IOSTA2	IOSTA1	IOSTA0

Read/Write-POR		W-1	W-1	W-1	W-1	W-1	W-1	W-1	W-1
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x06	IOSTB	IOSTB7	IOSTB6	IOSTB5	IOSTB4	IOSTB3	IOSTB2	IOSTB1	IOSTB0

Accessed by IOST instruction.
Note: more bits' default state, please refer to Table 2.2.

The Port I/O Control Registers are loaded with the contents of the ACC Register by executing the IOST R (0x05~0x06) instruction.
The IOST Registers are "write-only" and are set (output drivers disabled) upon RESET.

IOSTA3:IOSTA0: PORTA I/O control bit.
= 0, PORTA pin configured as an output.
= 1, PORTA pin configured as an input (tri-stated).

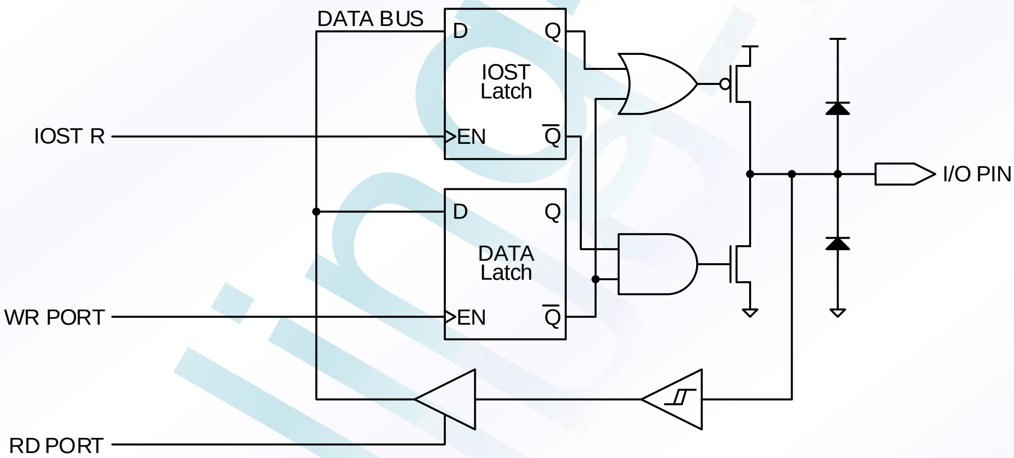
IOSTB7:IOSTB0: PORTB I/O control bit.
= 0, PORTB pin configured as an output.
= 1, PORTB pin configured as an input (tri-stated).
Note: 1. IOB3 is open-drain output only if IOSTB3 = 0.
2. ***The IOB3 open-drain function will be fixed to "Disable" by H/W if the configuration bit IOB3OD= Disable, even if bit IOSTB3 = 0.***

2.2 I/O Ports

Port A and port B are bi-directional tristate I/O ports. Port A is a 4-pin I/O port. Port B is an 8-pin I/O port. Please note that IOB3 is an input or open-drain output pin.
All I/O pins have data direction control registers (IOSTA, IOSTB) which can configure these pins as output or input.
The exceptions are IOB2 which may be controlled by the T0CS bit (OPTION<5>).
IOB<5:4> and IOB<2:0> have its corresponding pull-high control bits (PHCON register) to enable the weak internal pull-high. The weak pull-high is automatically turned off when the pin is configured as an output pin.
IOA<3:0> and IOB<2:0> have its corresponding pull-down control bits (PDCON register) to enable the weak internal pull-down. The weak pull-down is automatically turned off when the pin is configured as an output pin.
IOB<7:4> and IOB<2:0> have its corresponding open-drain control bits (ODCON register) to enable the open-drain output when these pins are configured to be an output pin.
IOB<7:0> also provides the input change interrupt/wake-up function. Each pin has its corresponding input change interrupt/wake-up enable bits (WUCON) to select the input change interrupt/wake-up source.
The IOB0 is also an external interrupt input signal by setting the EIS bit (PCON<6>). In this case, IOB0 input change interrupt/wake-up function will be disabled by hardware even if it is enabled by software.
The CONFIGURATION words can set several I/Os to alternate functions. When acting as alternate functions the pins will read as “0” during port read.

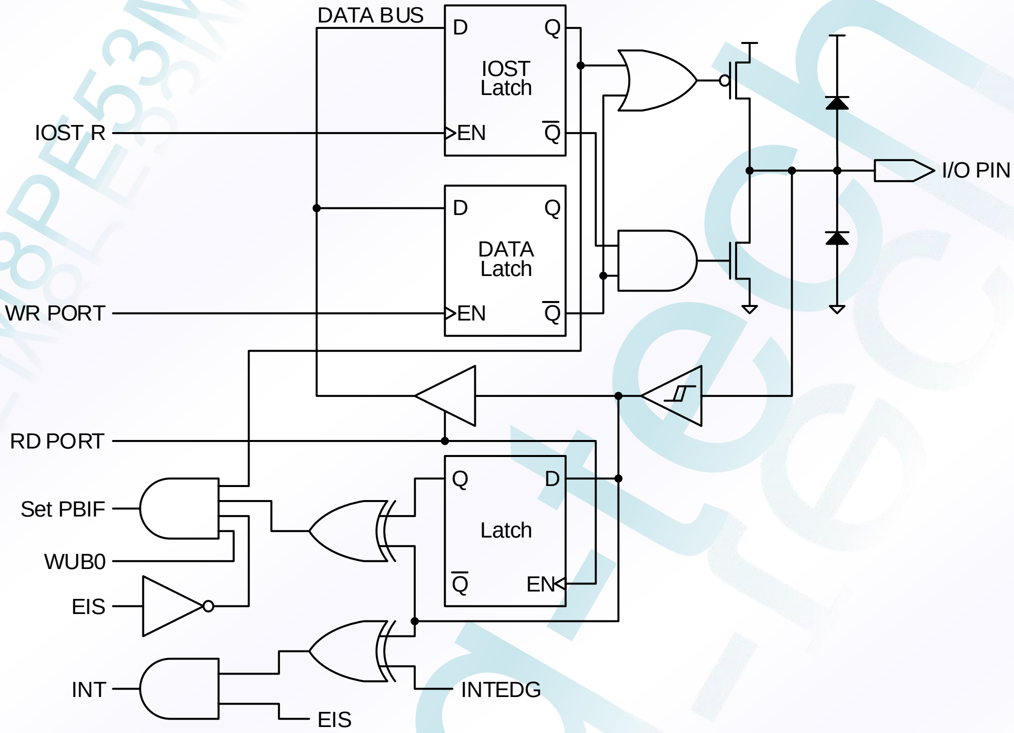
Figure 2.3: Block Diagram of I/O Pins

IOA3 ~ IOA0:



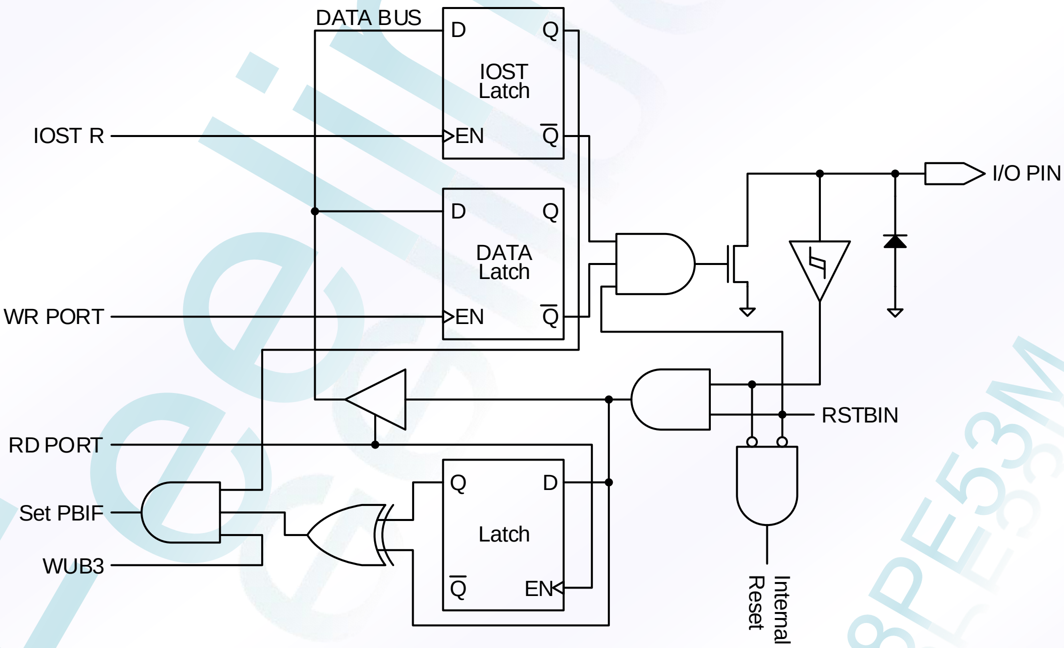
Pull-down is not shown in the figure

IOB0/INT:



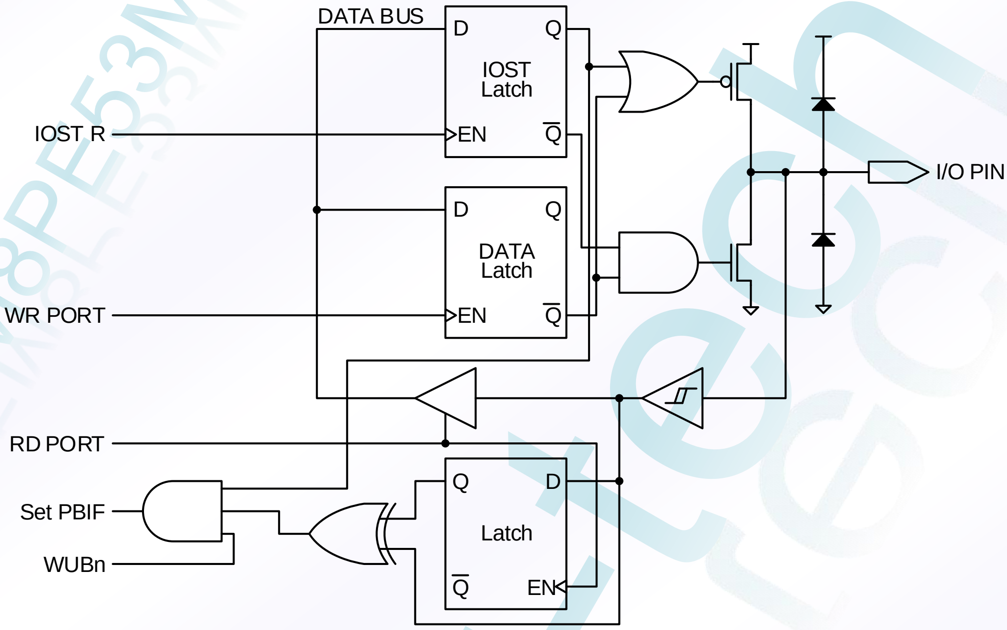
Pull-high/pull-down and open-drain are not shown in the figure

IOB3:



Voltage on this pin must not exceed V_{DD}.

IOB7 ~ IOB4, IOB2 ~ IOB1:



Pull-high/pull-down and open-drain are not shown in the figure

2.3 Timer0/WDT & Pre-scler

2.3.1 Timer0

The Timer0 is an 8-bit timer/counter. The clock source of Timer0 can come from the internal clock or by an external clock source (T0CKI pin).

2.3.1.1 Using Timer0 with an Internal Clock: Timer mode

Timer mode is selected by clearing the T0CS bit (OPTION<5>). In timer mode, the timer0 register (TMR0) will increment every instruction cycle (without pre-scaler). If TMR0 register is written, the increment is inhibited for the following two cycles.

2.3.1.2 Using Timer0 with an External Clock: Counter mode

Counter mode is selected by setting the T0CS bit (OPTION<5>). In this mode, Timer0 will increment either on every rising or falling edge of pin T0CKI. The incrementing edge is determined by the source edge select bit T0SE (OPTION<4>).
The external clock requirement is due to internal phase clock (T_{OSC}) synchronization. Also, there is a delay in the actual incrementing of Timer0 after synchronization.
When no pre-scaler is used, the external clock input is the same as the pre-scaler output. The synchronization of T0CKI with the internal phase clocks is accomplished by sampling the pre-scaler output on the T2 and T4 cycles of the internal phase clocks. Therefore, it is necessary for T0CKI to be high for at least 2 T_{OSC} and low for at least 2 T_{OSC}.
When a pre-scaler is used, the external clock input is divided by the asynchronous pre-scaler. For the external clock to meet the sampling requirement, the ripple counter must be taken into account. Therefore, it is necessary for T0CKI to have a period of at least 4 T_{OSC} divided by the pre-scaler value.

2.3.2 Watchdog Timer (WDT)

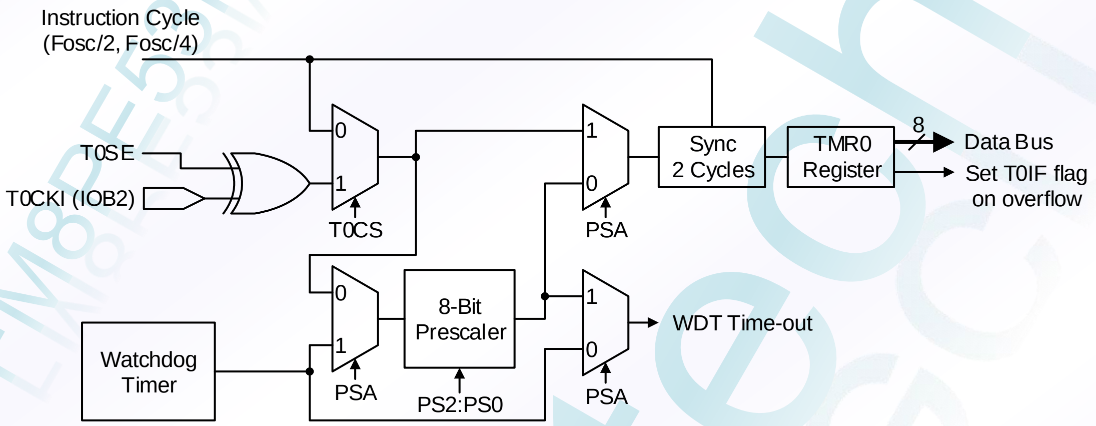
The Watchdog Timer (WDT) is a free running on-chip RC oscillator which does not require any external components. So the WDT will still run even if the clock on the OSCI and OSCO pins is turned off, such as in SLEEP mode. During normal operation or in SLEEP mode, a WDT time-out will cause the device reset and the $\overline{\text{TO}}$ bit (STATUS<4>) will be cleared.
The WDT can be disabled by clearing the control bit WDTE (PCON<7>) to "0".
The WDT has a nominal time-out period of 18ms, 4.5ms, 288ms or 72ms selected by SUT bit of configuration word (without pre-scaler). If a longer time-out period is desired, a pre-scaler with a division ratio of up to 1:128 can be assigned to the WDT controlled by the OPTION register. Thus, the longest time-out period is approximately 36.8 seconds.
The CLRWDT instruction clears the WDT and the pre-scaler, if assigned to the WDT, and prevents it from timing out and generating a device reset.
The SLEEP instruction resets the WDT and the pre-scaler, if assigned to the WDT. This gives the maximum SLEEP time before a WDT Wake-up Reset.

2.3.3 Pre-scaler

An 8-bit counter (down counter) is available as a pre-scaler for the Timer0, or as a post-scaler for the Watchdog Timer (WDT). Note that the pre-scaler may be used by either the Timer0 module or the WDT, but not both. Thus, a pre-scaler assignment for the Timer0 means that there is no pre-scaler for the WDT, and vice-versa.
The PSA bit (OPTION<3>) determines pre-scaler assignment. The PS<2:0> bits (OPTION<2:0>) determine pre-scaler ratio.
When the pre-scaler is assigned to the Timer0 module, all instructions writing to the TMR0 register will clear the pre-scaler. When it is assigned to WDT, a CLRWDT instruction will clear the pre-scaler along with the WDT.
The pre-scaler is neither readable nor writable. On a RESET, the pre-scaler contains all '1's.
To avoid an unintended device reset, CLRWDT or CLRR TMR0 instructions must be executed when changing the

pre-scaler assignment from Timer0 to the WDT, and vice-versa.

Figure 2.4: Block Diagram of the Timer0/WDT Pre-scaler



2.4 Interrupts

The FM8PE53M has up to three sources of interrupt:
1. External interrupt INT pin.
2. TMR0 overflow interrupt.
3. Port B input change interrupt (pins IOB7:IOB0).

INTFLAG is the interrupt flag register that recodes the interrupt requests in the relative flags.
A global interrupt enable bit, GIE (INTEN<7>), enables (if set) all un-masked interrupts or disables (if cleared) all interrupts. Individual interrupts can be enabled/disabled through their corresponding enable bits in INTEN register regardless of the status of the GIE bit.
When an interrupt event occurs with the GIE bit and its corresponding interrupt enable bit are all set, the GIE bit will be cleared by hardware to disable any further interrupts, and the next instruction will be fetched from address 0x008.
The interrupt flag bits must be cleared by software before re-enabling GIE bit to avoid recursive interrupts.
The RETFIE instruction exits the interrupt routine and set the GIE bit to re-enable interrupt.
The flag bit (except PBIF bit) in INTFLAG register is set by interrupt event regardless of the status of its mask bit.
Reading the INTFLAG register will be the logic AND of INTFLAG and INTEN.
When an interrupt is generated by the INT instruction, the next instruction will be fetched from address 0x002.

2.4.1 External INT Interrupt

External interrupt on INT pin is rising or falling edge triggered selected by INTEDG (OPTION<6>).
When a valid edge appears on the INT pin the flag bit INTIF (INTFLAG<2>) is set. This interrupt can be disabled by clearing INTIE bit (INTEN<2>).
The INT pin interrupt can wake-up the system from SLEEP condition, if bit INTIE was set before going to SLEEP. If GIE bit was set, the program will execute interrupt service routine after wake-up; or if GIE bit was cleared, the program will execute next PC after wake-up.

2.4.2 Timer0 Interrupt

An overflow (0xFF → 0x00) in the TMR0 register will set the flag bit T0IF (INTFLAG<0>). This interrupt can be disabled by clearing T0IE bit (INTEN<0>).

2.4.3 Port B Input Change Interrupt

An input change on IOB<7:0> set flag bit PBIF (INTFLAG<1>). This interrupt can be disabled by clearing PBIE bit (INTEN<1>).

Before the port B input change interrupt is enabled, reading PORTB (any instruction accessed to PORTB, including read/write instructions) is necessary. Any pin which corresponding WUBn bit (WUCON<5:0>) is cleared to "0" or configured as output or IOB0 pin configured as INT pin will be excluded from this function.
The port B input change interrupt also can wake-up the system from SLEEP condition, if bit PBIE was set before going to SLEEP. And GIE bit also decides whether or not the processor branches to the interrupt vector following wake-up. If GIE bit was set, the program will execute interrupt service routine after wake-up; or if GIE bit was cleared, the program will execute next PC after wake-up.

2.5 Power-down Mode (SLEEP)

Power-down mode is entered by executing a SLEEP instruction.
When SLEEP instruction is executed, the $\overline{PD}$ bit (STATUS<3>) is cleared, the $\overline{TO}$ bit is set, the watchdog timer will be cleared and keeps running, and the oscillator driver is turned off.
All I/O pins maintain the status they had before the SLEEP instruction was executed.

2.5.1 Wake-up from SLEEP Mode

The device can wake-up from SLEEP mode through one of the following events:
1. RSTB reset.
2. WDT time-out reset (if enabled).
3. Interrupt from IOB0/INT pin, or PORTB change interrupt.

External RSTB reset and WDT time-out reset will cause a device reset. The $\overline{PD}$ and $\overline{TO}$ bits can be used to determine the cause of device reset. The $\overline{PD}$ bit is set on power-up and is cleared when SLEEP instruction is executed. The $\overline{TO}$ bit is cleared if a WDT time-out occurred.
For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set. Wake-up is regardless of the GIE bit. If GIE bit is cleared, the device will continue execution at the instruction after the SLEEP instruction. If the GIE bit is set, the device will branch to the interrupt address (0x008).
In HF, XT or LF oscillation mode, the system wake-up delay time is 18/4.5/288/72ms (selected by SUT bit of configuration word).
And in IRC or ERIC oscillation mode, the system wake-up delay time is 140us.

2.6 Reset

FM8PE53M devices may be RESET in one of the following ways:
1. Power-on Reset (POR)
2. Brown-out Reset (BOR)
3. RSTB Pin Reset
4. WDT time-out Reset

Some registers are not affected in any RESET condition. Their status is unknown on Power-on Reset and unchanged in any other RESET. Most other registers are reset to a "reset state" on Power-on Reset, RSTB or WDT Reset.
A Power-on RESET pulse is generated on-chip when V_{DD} rise is detected. To use this feature, the user merely ties the RSTB pin to V_{DD}.
On-chip Low Voltage Detector (LVD) places the device into reset when V_{DD} is below a fixed voltage. This ensures that the device does not continue program execution outside the valid operation V_{DD} range. Brown-out RESET is typically used in AC line or heavy loads switched applications.
A RSTB or WDT Wake-up from SLEEP also results in a device RESET, and not a continuation of operation before SLEEP.
The $\overline{TO}$ and $\overline{PD}$ bits (STATUS<4:3>) are set or cleared depending on the different reset conditions.

2.6.1 Power-up Reset Timer (PWRT)

The Power-up Reset Timer provides a nominal 18/4.5/288/72ms (selected by SUT bit of configuration word) (or 140us, varies based on oscillator selection and reset condition) delay after Power-on Reset (POR), Brown-out Reset

(BOR), RSTB Reset or WDT time-out Reset. The device is kept in reset state as long as the PWRT is active. The PWDT delay will vary from device to device due to V_{DD}, temperature, and process variation.

Table 2.1: PWRT Period

Oscillator Mode	Power-on Reset Brown-out Reset	RSTB Reset WDT time-out Reset
IRC & ERC & ERIC	18/4.5/288/72ms or 140us	140us
HF & XT & LF	18/4.5/288/72ms	18/4.5/288/72ms

2.6.2 Oscillator Start-up Timer (OST)

The OST timer provides a 64-oscillator cycle delay (from OSCI input) after the PWRT delay (18/4.5/288/72ms or 140us) is over. This delay ensures that the oscillator has started and stabilized. The device is kept in reset state as long as the OST is active.
This counter only starts incrementing after the amplitude of the OSCI signal reaches the oscillator input thresholds.

2.6.3 Reset Sequence

When Power-on Reset (POR), Brown-out Reset (BOR), RSTB Reset or WDT time-out Reset is detected, the reset sequence is as follows:

1. The reset latch is set and the PWRT & OST are cleared.
2. When the internal POR, BOR, RSTB Reset or WDT time-out Reset pulse is finished, then the PWRT begins counting.
3. After the PWRT time-out, the OST is activated.
4. And after the OST delay is over, the reset latch will be cleared and thus end the on-chip reset signal.

In HF, XT or LF oscillation mode, the totally system reset delay time is 18/4.5/288/72ms plus 64 oscillator cycle time. And in IRC/ERIC or ERC oscillation mode, the totally system reset delay time is 18/4.5/288/72ms or 140us after Power-on Reset (POR), Brown-out Reset (BOR), or 140us after RSTB Reset or WDT time-out Reset.

Figure 2.5: Simplified Block Diagram of on-chip Reset Circuit

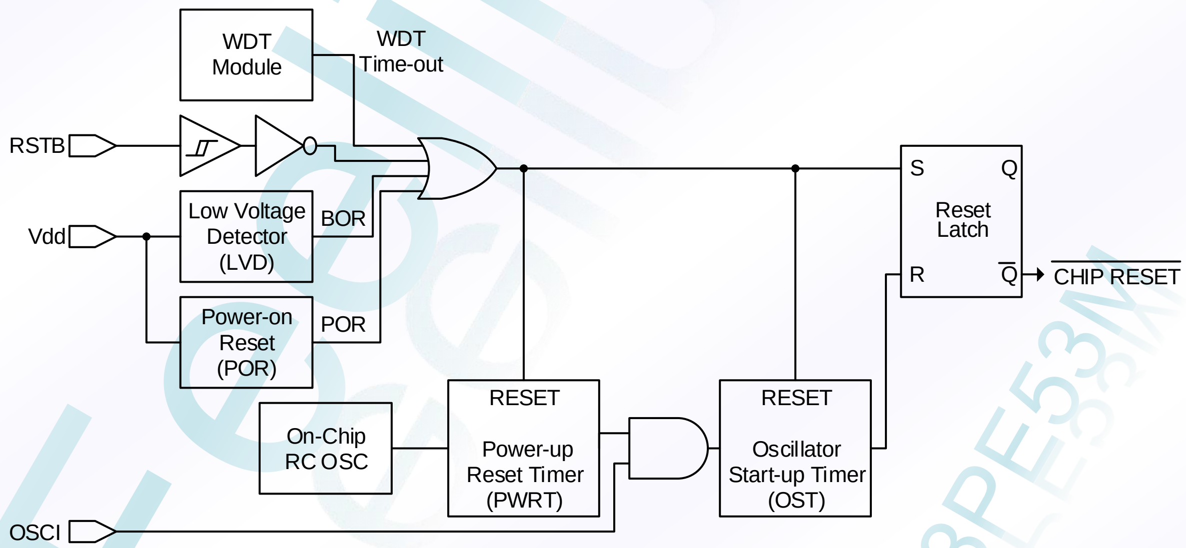


Table 2.2: Reset Conditions for All Registers

Register	Address	Power-on Reset Brown-out Reset	RSTB Reset WDT Reset
ACC	N/A	xxxx xxxx	uuuu uuuu
OPTION	N/A	*011 1111	*011 1111
IOSTA	0x05	---- 1111	---- 1111
IOSTB	0x06	1111 1111	1111 1111
INDF	0x00	xxxx xxxx	uuuu uuuu
TMR0	0x01	xxxx xxxx	uuuu uuuu
PCL	0x02	1111 1111	1111 1111
STATUS	0x03	0001 1xxx	000# #uuu
FSR	0x04	**xx xxxx	**uu uuuu
PORTA	0x05	xxxx xxxx	uuuu uuuu
PORTB	0x06	xxxx xxxx	uuuu uuuu
General Purpose Register	0x07	xxxx xxxx	uuuu uuuu
PCON	0x08	101* ****	101* ****
WUCON	0x09	0000 0000	0000 0000
PCHBUF	0x0A	---- --11	---- --11
PDCON	0x0B	1111 1111	1111 1111
ODCON	0x0C	0000 0000	0000 0000
PHCON	0x0D	1111 1111	1111 1111
INTEN	0x0E	0*** *000	0*** *000
INTFLAG	0x0F	---- -000	---- -000
General Purpose Registers	0x10 ~ 0x3F	xxxx xxxx	uuuu uuuu

Legend: u = unchanged, x = unknown, - = unimplemented, read as ‘0’; * = unimplemented, read as ‘1’; # = refer to the following table for possible values.

Table 2.3: RST / $\overline{TO}$ / $\overline{PD}$ Status after Reset or Wake-up

RST	$\overline{TO}$	$\overline{PD}$	RESET was caused by
0	1	1	Power-on Reset.
0	1	1	Brown-out reset.
0	u	u	RSTB Reset during normal operation.
0	1	0	RSTB Reset during SLEEP.
0	0	1	WDT Reset during normal operation.
0	0	0	WDT Wake-up during SLEEP.
1	1	0	Wake-up on pin change during SLEEP.

Legend: u = unchanged

Table 2.4: Events Affecting$\overline{TO}$ / $\overline{PD}$Status Bits

Event	$\overline{TO}$	$\overline{PD}$
Power-on.	1	1
WDT Time-Out.	0	u
SLEEP instruction.	1	0
CLRWDT instruction.	1	1

Legend: u = unchanged.

2.7 Hexadecimal Convert to Decimal (HCD)

Decimal format is another number format for FM8PE53M. When the content of the data memory has been assigned as decimal format, it is necessary to convert the results to decimal format after the execution of ALU instructions. When the decimal converting, operation is processing, all of the operand data (including the contents of the data memory (RAM), accumulator (ACC), immediate data, and look-up table) should be in the decimal format, or the results of conversion will be incorrect.
Instruction DAA can convert the ACC data from hexadecimal to decimal format after any addition operation and restored to ACC.
The conversion operation is illustrated in example 2.2.

Example 2.2: DAA CONVERSION

Code
```
#include    <8PE53M.ASH>
            …
            MOVIA     0x90       ;Set immediate data = decimal format number "90" (ACC ← 0x90)
            MOVAR     0x30       ;Load immediate data "90" to data memory address 0x30
            MOVIA     0x10       ;Set immediate data = decimal format number "10" (ACC ← 0x10)
            ADDAR     0x30,A     ;Contents of the data memory address 0x30 and ACC are binary-added
                                 ;the result loads to the ACC (ACC ← 0xA0, C ← 0)
            DAA                  ;Convert the content of ACC to decimal format, and restored to ACC
                                 ;The result in the ACC is "00" and the carry bit C is "1". This represents the
                                 ;decimal number "100"
            …
```

Instruction DAS can convert the ACC data from hexadecimal to decimal format after any subtraction operation and restored to ACC.
The conversion operation is illustrated in example 2.3.

Example 2.3: DAS CONVERSION

Code
```
#include    <8PE53M.ASH>
            …
            MOVIA     0x10       ;Set immediate data = decimal format number "10" (ACC ← 0x10)
            MOVAR     0x30       ;Load immediate data "90" to data memory address 0x30
            MOVIA     0x20       ;Set immediate data = decimal format number "20" (ACC ← 0x20)
            SUBAR     0x30,A     ;Contents of the data memory address 0x30 and ACC are binary-subtracted
                                 ;the result loads to the ACC (ACC ← 0xF0, C ← 0)
            DAS                  ;Convert the content of ACC to decimal format, and restored to ACC
                                 ;The result in the ACC is "90" and the carry bit C is "0". This represents the
                                 ;decimal number " -10"
            …
```

2.8 Oscillator Configurations

FM8PE53M can be operated in six different oscillator modes. Users can program F_{OSC} configuration bit to select the appropriate modes:

- ERC: External Resistor/Capacitor Oscillator
- HF: High Frequency Crystal/Resonator Oscillator
- XT: Crystal/Resonator Oscillator
- LF: Low Frequency Crystal Oscillator
- IRC: Internal Resistor/Capacitor Oscillator
- ERIC: External Resistor/Internal Capacitor Oscillator

In LF, XT, or HF modes, a crystal or ceramic resonator in connected to the OSCI and OSCO pins to establish oscillation. When in LF, XT, or HF modes, the devices can have an external clock source drive the OSCI pin.
The ERC device option offers additional cost savings for timing insensitive applications. The RC oscillator frequency is a function of the resistor (R_{EXT}) and capacitor (C_{EXT}), the operating temperature, and the process parameter.
The IRC/ERIC device option offers largest cost savings for timing insensitive applications. These devices offer 4 different internal RC oscillator frequency, 8MHZ, 4MHZ, 1MHZ, and 455KHZ, which is selected by configuration bit (F_{OSC}). Or user can change the oscillator frequency with external resistor. The ERIC oscillator frequency is a function of the resistor (R_{EXT}), the operating temperature, and the process parameter.

Figure 2.6: HF, XT or LF Oscillator Modes (Crystal Operation or Ceramic Resonator)

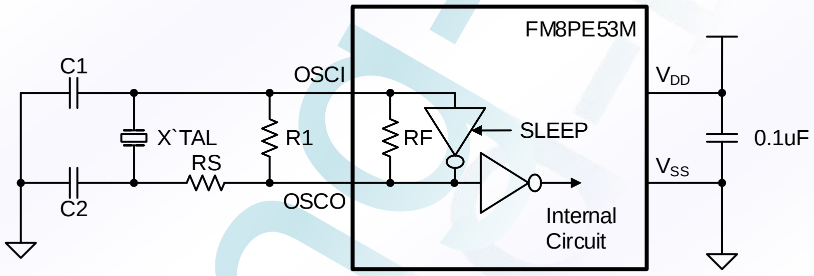


Figure 2.7: HF, XT or LF Oscillator Modes (External Clock Input Operation)

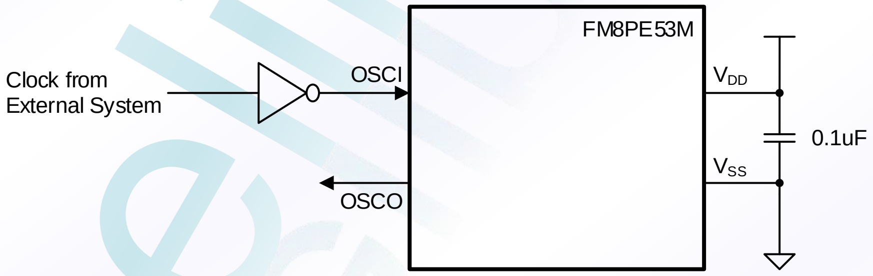


Figure 2.8: ERC Oscillator Mode (External RC Oscillator)

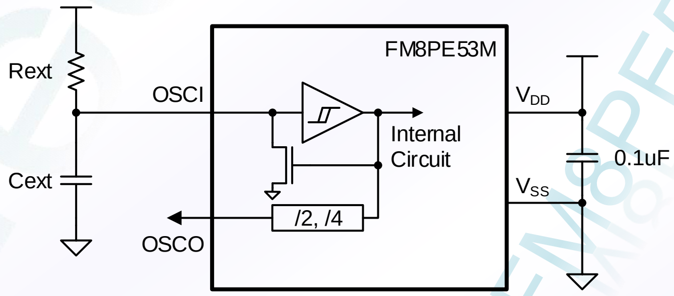
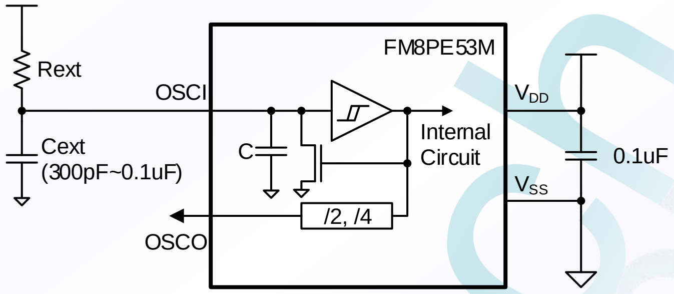


Figure 2.9: ERIC Oscillator Mode (External R, Internal C Oscillator)

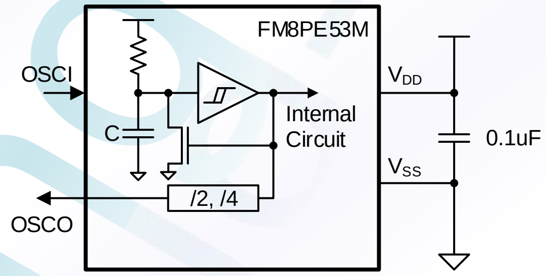


The typical oscillator frequency vs. external resistor is as following table
When C_{EXT} = 0.01uf (103)

Frequency	R_{EXT} @ 3V	R_{EXT} @ 5V
455KHZ	958.7K	1.45M
1MHZ	691.2K	933.2K
4MHZ	280.2K	322.6K
8MHZ	158.1K	167.7K

Note: Values are provided for design reference only.

Figure 2.10: IRC Oscillator Mode (Internal R, Internal C Oscillator)



2.9 Configuration Words

Table 2.5: Configuration Words

Name	Description
F_{OSC}	Oscillator Selection Bit → ERC mode (external R & C) (default) IOB4/OSCO pin controlled by OSCOUT configuration bit → HF mode → XT mode → LF mode → 4MHZ IRC mode (internal R & C) IOB4/OSCO pin controlled by OSCOUT configuration bit → 8MHZ IRC mode (internal R & C) IOB4/OSCO pin controlled by OSCOUT configuration bit → 1MHZ IRC mode (internal R & C) IOB4/OSCO pin controlled by OSCOUT configuration bit → 455KHZ IRC mode (internal R & C) IOB4/OSCO pin controlled by OSCOUT configuration bit → ERIC mode (external R & internal C) IOB4/OSCO pin controlled by OSCOUT configuration bit Note: See Table 2.6 for detail description.
LVDT	Low Voltage Detector Selection Bit → Enable, LVDT voltage = 3.6V → Enable, LVDT voltage = 2.6V → Enable, LVDT voltage = 2.4V → Enable, LVDT voltage = 2.2V → Enable, LVDT voltage = 2.0V → Enable, LVDT voltage = 2.0V, controlled by SLEEP → Enable, LVDT voltage = 1.8V → Disable (default)
SUT	PWRT & WDT Time Period Selection Bit (The value must be a multiple of pre-scaler rate) → PWRT = WDT pre-scaler rate = 18ms (default) → PWRT = WDT pre-scaler rate = 4.5ms → PWRT = WDT pre-scaler rate = 288ms → PWRT = WDT pre-scaler rate = 72ms → PWRT = 140us, WDT pre-scaler rate = 18ms → PWRT = 140us, WDT pre-scaler rate = 4.5ms → PWRT = 140us, WDT pre-scaler rate = 288ms → PWRT = 140us, WDT pre-scaler rate = 72ms
OSCOUT	IOB4/OSCO Pin Selection Bit for IRC/ERIC Mode → OSCO pin is selected (default) → IOB4 pin is selected
RSTBIN	IOB3/RSTB Pin Selection Bit → IOB3 pin is selected (default) → RSTB pin is selected
WDTEN	Watchdog Timer Enable Bit → WDT enabled (default) → WDT disabled
PROTECT	Code Protection Bit → OTP code protection off (default) → OTP code protection on
OSCD	Instruction Period Selection Bit → Four oscillator periods (default) → Two oscillator periods

Name	Description
RDPORT	Read Port Control Bit for Output Pins → From registers (default) → From pins
SCHMITT	I/O Pin Input Buffer Control Bit → With Schmitt-trigger (default) → Without Schmitt-trigger
IOB3OD	IOB3 Pin Open-Drain Output Enable Bit → Enable open-drain function (IOB3 pin is Bi-direction) (default) → Disable open-drain function (IOB3 pin is Only input)

Table 2.6: Selection of IOB5/OSCI and IOB4/OSCO Pins

Mode of oscillation	IOB5/OSCI	IOB4/OSCO
IRC	Force to IOB5	IOB4/OSCO selected by OSCOUT bit
ERC, ERIC	Force to OSCI	IOB4/OSCO selected by OSCOUT bit
HF, XT, LF	Force to OSCI	Force to OSCO

3.0 INSTRUCTION SET

Mnemonic, Operands		Description	Operation	Cycles	Status Affected
BCR	**R, bit**	Clear bit in R	0 → R<b>	1	-
BSR	**R, bit**	Set bit in R	1 → R<b>	1	-
BTRSC	**R, bit**	Test bit in R, Skip if Clear	Skip if R<b> = 0	1/2(1)	-
BTRSS	**R, bit**	Test bit in R, Skip if Set	Skip if R<b> = 1	1/2(1)	-
NOP		No Operation	No operation	1	-
CLRWDT		Clear Watchdog Timer	0x00 → WDT, 0x00 → WDT pre-scaler	1	$\overline{TO}$, $\overline{PD}$
SLEEP		Go into power-down mode	0x00 → WDT, 0x00 → WDT pre-scaler	1	$\overline{TO}$, $\overline{PD}$
OPTION		Load OPTION register	ACC → OPTION	1	-
DAA		Adjust ACC's data format from HEX to DEC after any addition operation	ACC(hex) → ACC (Dec)	1	C
DAS		Adjust ACC's data format from HEX to DEC after any subtraction operation	ACC(hex) → ACC (Dec)	1	-
RETURN		Return from subroutine	Top of Stack → PC	2	-
RETFIE		Return from interrupt, set GIE bit	Top of Stack → PC, 1 → GIE	2	-
INT		S/W interrupt	PC + 1 → Top of Stack 0x002 → PC	2	-
IOST	**R**	Load IOST register	ACC → IOST register	1	-
CLRA		Clear ACC	0x00 → ACC	1	Z
CLRR	**R**	Clear R	0x00 → R	1	Z
MOVAR	**R**	Move ACC to R	ACC → R	1	-
MOVR	**R, d**	Move R	R → dest	1	Z
DECR	**R, d**	Decrement R	R - 1 → dest	1	Z
DECRSZ	**R, d**	Decrement R, Skip if 0	R - 1 → dest, Skip if result = 0	1/2(1)	-
INCR	**R, d**	Increment R	R + 1 → dest	1	Z
INCRSZ	**R, d**	Increment R, Skip if 0	R + 1 → dest, Skip if result = 0	1/2(1)	-
ADDAR	**R, d**	Add ACC and R	R + ACC → dest	1	C, DC, Z
SUBAR	**R, d**	Subtract ACC from R	R - ACC → dest	1	C, DC, Z
ADCAR	**R, d**	Add ACC and R with Carry	R + ACC + C → dest	1	C, DC, Z
SBCAR	**R, d**	Subtract ACC from R with Carry	R + $\overline{ACC}$ + C → dest	1	C, DC, Z
ANDAR	**R, d**	AND ACC with R	ACC and R → dest	1	Z
IORAR	**R, d**	Inclusive OR ACC with R	ACC or R → dest	1	Z
XORAR	**R, d**	Exclusive OR ACC with R	R xor ACC → dest	1	Z
COMR	**R, d**	Complement R	$\overline{R}$ → dest	1	Z
RLR	**R, d**	Rotate left R through Carry	R<7> → C, R<6:0> → dest<7:1>, C → dest<0>	1	C
RRR	**R, d**	Rotate right R through Carry	C → dest<7>, R<7:1> → dest<6:0>, R<0> → C	1	C
SWAPR	**R, d**	Swap R	R<3:0> → dest<7:4>, R<7:4> → dest<3:0>	1	-

Mnemonic, Operands		Description	Operation	Cycles	Status Affected
MOVIA	**I**	Move Immediate to ACC	I → ACC	1	-
ADDIA	**I**	Add ACC and Immediate	I + ACC → ACC	1	C, DC, Z
SUBIA	**I**	Subtract ACC from Immediate	I - ACC → ACC	1	C, DC, Z
ANDIA	**I**	AND Immediate with ACC	ACC and I → ACC	1	Z
IORIA	**I**	OR Immediate with ACC	ACC or I → ACC	1	Z
XORIA	**I**	Exclusive OR Immediate to ACC	ACC xor I → ACC	1	Z
RETIA	**I**	Return, place Immediate in ACC	I → ACC, Top of Stack → PC	2	-
CALL	**I**	Call subroutine	PC + 1 → Top of Stack, I → PC	2	-
GOTO	**I**	Unconditional branch	I → PC	2	-

Note: 1. 2 cycles for skip, else 1 cycle.
2. bit:Bit address within an 8-bit register R
R:Register address (0x00 to 0x3F)
I:Immediate data
ACC:Accumulator
d:Destination select;
=0 (store result in ACC)
=1 (store result in file register R)
dest:Destination
PC:Program Counter
PCH:High Byte register of Program Counter
WDT:Watchdog Timer Counter
GIE:Global interrupt enable bit
$\overline{TO}$:Time-out bit
$\overline{PD}$:Power-down bit
C:Carry bit
DC:Half carry bit
Z:Zero bit

ADCAR	**Add ACC and R with Carry**
Syntax:	ADCAR R, d
Operands:	0x00≤R≤0x3F d∈[0,1]
Operation:	R + ACC + C → dest
Status Affected:	C, DC, Z
Description:	Add the contents of the ACC register and register 'R' with Carry. If 'd' is 0 the result is stored in the ACC register. If 'd' is '1' the result is stored back in register 'R'.
Cycles:	1

ADDAR	**Add ACC and R**
Syntax:	ADDAR R, d
Operands:	0x00≤R≤0x3F d∈[0,1]
Operation:	ACC + R → dest
Status Affected:	C, DC, Z
Description:	Add the contents of the ACC register and register 'R'. If 'd' is 0 the result is stored in the ACC register. If 'd' is '1' the result is stored back in register 'R'.
Cycles:	1

ADDIA	**Add ACC and Immediate**
Syntax:	ADDIA I
Operands:	0x00≤I≤0xFF
Operation:	ACC + I → ACC
Status Affected:	C, DC, Z
Description:	Add the contents of the ACC register with the 8-bit immediate 'I'. The result is placed in the ACC register.
Cycles:	1

ANDAR	**AND ACC and R**
Syntax:	ANDAR R, d
Operands:	0x00≤R≤0x3F d∈[0,1]
Operation:	ACC and R → dest
Status Affected:	Z
Description:	The contents of the ACC register are AND'ed with register 'R'. If 'd' is 0 the result is stored in the ACC register. If 'd' is '1' the result is stored back in register 'R'.
Cycles:	1

ANDIA	**AND Immediate with ACC**
Syntax:	ANDIA I
Operands:	0x00≤I≤0xFF
Operation:	ACC AND I → ACC
Status Affected:	Z
Description:	The contents of the ACC register are AND'ed with the 8-bit immediate 'I'. The result is placed in the ACC register.
Cycles:	1

BCR	**Clear Bit in R**
Syntax:	BCR R, b
Operands:	0x00≤R≤0x3F 0x0≤b≤0x7
Operation:	0 → R<b>
Status Affected:	None
Description:	Clear bit ‘b’ in register ‘R’.
Cycles:	1

BSR	**Set Bit in R**
Syntax:	BSR R, b
Operands:	0x00≤R≤0x3F 0x0≤b≤0x7
Operation:	1 → R<b>
Status Affected:	None
Description:	Set bit ‘b’ in register ‘R’.
Cycles:	1

BTRSC	**Test Bit in R, Skip if Clear**
Syntax:	BTRSC R, b
Operands:	0x00≤R≤0x3F 0x0≤b≤0x7
Operation:	Skip if R<b> = 0
Status Affected:	None
Description:	If bit ‘b’ in register ‘R’ is 0 then the next instruction is skipped. If bit ‘b’ is 0 then next instruction fetched during the current instruction execution is discarded, and a NOP is executed instead making this a 2-cycle instruction.
Cycles:	1/2

BTRSS	**Test Bit in R, Skip if Set**
Syntax:	BTRSS R, b
Operands:	0x00≤R≤0x3F 0x0≤b≤0x7
Operation:	Skip if R<b> = 1
Status Affected:	None
Description:	If bit ‘b’ in register ‘R’ is ‘1’ then the next instruction is skipped. If bit ‘b’ is ‘1’, then the next instruction fetched during the current instruction execution, is discarded and a NOP is executed instead, making this a 2-cycle instruction.
Cycles:	1/2

CALL	**Subroutine Call**
Syntax:	CALL I
Operands:	0x000≤I≤0x3FF
Operation:	PC + 1 → Top of Stack, I → PC<9:0>
Status Affected:	None
Description:	Subroutine call. First, return address (PC+1) is pushed onto the stack. The 10-bit immediate address is loaded into PC bits <9:0>.
Cycles:	2

CLRA	**Clear ACC**
Syntax:	CLRA
Operands:	None
Operation:	0x00 → ACC; 1 → Z
Status Affected:	Z
Description:	The ACC register is cleared. Zero bit (Z) is set.
Cycles:	1

CLRR	**Clear R**
Syntax:	CLRR R
Operands:	0x00≤R≤0x3F
Operation:	0x00 → R; 1 → Z
Status Affected:	Z
Description:	The contents of register 'R' are cleared and the Z bit is set.
Cycles:	1

CLRWDT	**Clear Watchdog Timer**
Syntax:	CLRWDT
Operands:	None
Operation:	0x00 → WDT; 0x00 → WDT pre-scaler (if assigned); 1 → $\overline{TO}$; 1 → $\overline{PD}$
Status Affected:	$\overline{TO}$, $\overline{PD}$
Description:	The CLRWDT instruction resets the WDT. It also resets the pre-scaler, if the pre-scaler is assigned to the WDT and not Timer0. Status bits $\overline{TO}$ and $\overline{PD}$ are set.
Cycles:	1

COMR	**Complement R**
Syntax:	COMR R, d
Operands:	0x00≤R≤0x3F d∈[0,1]
Operation:	$\overline{R}$→ dest
Status Affected:	Z
Description:	The contents of register 'R' are complemented. If 'd' is 0 the result is stored in the ACC register. If 'd' is 1 the result is stored back in register 'R'.
Cycles:	1

DAA	**Adjust ACC's data format from HEX to DEC**
Syntax:	DAA
Operands:	None
Operation:	ACC(hex) → ACC(dec)
Status Affected:	C
Description:	Convert the ACC data from hexadecimal to decimal format after any addition operation and restored to ACC.
Cycles:	1

DAS	**Adjust ACC's data format from HEX to DEC**
Syntax:	DAS
Operands:	None
Operation:	ACC(hex) → ACC(dec)
Status Affected:	None
Description:	Convert the ACC data from hexadecimal to decimal format after any subtraction operation and restored to ACC.
Cycles:	1

DECR	**Decrement R**
Syntax:	DECR R, d
Operands:	0x00≤R≤0x3F d∈[0,1]
Operation:	R - 1 → dest
Status Affected:	Z
Description:	Decrement of register 'R'. If 'd' is 0 the result is stored in the ACC register. If 'd' is 1 the result is stored back in register 'R'.
Cycles:	1

DECRSZ	**Decrement R, Skip if 0**
Syntax:	DECRSZ R, d
Operands:	0x00≤R≤0x3F d∈[0,1]
Operation:	R - 1 → dest; skip if result =0
Status Affected:	None
Description:	The contents of register 'R' are decrement. If 'd' is 0 the result is placed in the ACC register. If 'd' is 1 the result is stored back in register 'R'. If the result is 0, the next instruction, which is already fetched, is discarded and a NOP is executed instead and making it a 2-cycle instruction.
Cycles:	1/2

GOTO	**Unconditional Branch**
Syntax:	GOTO I
Operands:	0x000≤I≤0x3FF
Operation:	I → PC<9:0>
Status Affected:	None
Description:	GOTO is an unconditional branch. The 10-bit immediate value is loaded into PC bits <9:0>.
Cycles:	2

INCR	**Increment R**
Syntax:	INCR R, d
Operands:	0x00≤R≤0x3F d∈[0,1]
Operation:	R + 1 → dest
Status Affected:	Z
Description:	The contents of register 'R' are increment. If 'd' is 0 the result is placed in the ACC register. If 'd' is 1 the result is stored back in register 'R'.
Cycles:	1

INCRSZ	Increment R, Skip if 0
Syntax:	INCRSZ R, d
Operands:	0x00≤R≤0x3F d∈[0,1]
Operation:	R + 1 → dest, skip if result = 0
Status Affected:	None
Description:	The contents of register 'R' are increment. If 'd' is 0 the result is placed in the ACC register. If 'd' is the result is stored back in register 'R'. If the result is 0, then the next instruction, which is already fetched, is discarded and a NOP is executed instead and making it a 2-cycle instruction.
Cycles:	1/2

INT	S/W Interrupt
Syntax:	INT
Operands:	None
Operation:	PC + 1 → Top of Stack, 0x002 → PC
Status Affected:	None
Description:	Interrupt subroutine call. First, return address (PC+1) is pushed onto the stack. The address 0x002 is loaded into PC bits <9:0>.
Cycles:	2

IORAR	OR ACC with R
Syntax:	IORAR R, d
Operands:	0x00≤R≤0x3F d∈[0,1]
Operation:	ACC or R → dest
Status Affected:	Z
Description:	Inclusive OR the ACC register with register 'R'. If 'd' is 0 the result is placed in the ACC register. If 'd' is 1 the result is placed back in register 'R'.
Cycles:	1

IORIA	OR Immediate with ACC
Syntax:	IORIA I
Operands:	0x00≤I≤0x3F
Operation:	ACC or I → ACC
Status Affected:	Z
Description:	The contents of the ACC register are OR'ed with the 8-bit immediate 'I'. The result is placed in the ACC register.
Cycles:	1

IOST	Load IOST Register
Syntax:	IOST R
Operands:	R = 0x06
Operation:	ACC → IOST register R
Status Affected:	None
Description:	IOST register 'R' (R= 0x06) is loaded with the contents of the ACC register.
Cycles:	1

MOVAR	Move ACC to R
Syntax:	MOVAR R
Operands:	0x00≤R≤0x3F
Operation:	ACC → R
Status Affected:	None
Description:	Move data from the ACC register to register ‘R’.
Cycles:	1

MOVIA	Move Immediate to ACC
Syntax:	MOVIA I
Operands:	0x00≤I≤0xFF
Operation:	I → ACC
Status Affected:	None
Description:	The 8-bit immediate ‘I’ is loaded into the ACC register. The don’t cares will assemble as 0s.
Cycles:	1

MOVR	Move R
Syntax:	MOVR R, d
Operands:	0x00≤R≤0x3F d∈[0,1]
Operation:	R → dest
Status Affected:	Z
Description:	The contents of register ‘R’ is moved to destination ‘d’. If ‘d’ is 0, destination is the ACC register. If ‘d’ is 1, the destination is file register ‘R’. ‘d’ is 1 is useful to test a file register since status flag Z is affected.
Cycles:	1

NOP	No Operation
Syntax:	NOP
Operands:	None
Operation:	No operation
Status Affected:	None
Description:	No operation.
Cycles:	1

OPTION	Load OPTION Register
Syntax:	OPTION
Operands:	None
Operation:	ACC → OPTION
Status Affected:	None
Description:	The content of the ACC register is loaded into the OPTION register.
Cycles:	1

RETFIE	Return from Interrupt, Set ‘GIE’ Bit
Syntax:	RETFIE
Operands:	None
Operation:	Top of Stack → PC 1 → GIE
Status Affected:	None
Description:	The program counter is loaded from the top of the stack (the return address). The ‘GIE’ bit is set to 1. This is a 2-cycle instruction.
Cycles:	2

RETIA **Return with Immediate in ACC**

Syntax: RETIA I
Operands: 0x00≤I≤0xFF
Operation: I → ACC;
Top of Stack → PC
Status Affected: None
Description: The ACC register is loaded with the 8-bit immediate 'I'. The program counter is loaded from the top of the stack (the return address). This is a 2-cycle instruction.
Cycles: 2

RETURN **Return from Subroutine**

Syntax: RETURN
Operands: None
Operation: Top of Stack → PC
Status Affected: None
Description: The program counter is loaded from the top of the stack (the return address). This is a 2-cycle instruction.
Cycles: 2

RLR **Rotate Left R through Carry**

Syntax: RLR R, d
Operands: 0x00≤R≤0x3F
d∈[0,1]
Operation: R<7> → C;
R<6:0> → dest<7:1>;
C → dest<0>
Status Affected: C
Description: The contents of register 'R' are rotated left one bit to the left through the Carry Flag. If 'd' is 0 the result is placed in the ACC register. If 'd' is 1 the result is stored back in register 'R'.
Cycles: 1

RRR **Rotate Right R through Carry**

Syntax: RRR R, d
Operands: 0x00≤R≤0x3F
d∈[0,1]
Operation: C → dest<7>;
R<7:1> → dest<6:0>;
R<0> → C
Status Affected: C
Description: The contents of register 'R' are rotated one bit to the right through the Carry Flag. If 'd' is 0 the result is placed in the ACC register. If 'd' is 1 the result is placed back in register 'R'.
Cycles: 1

SLEEP	**Enter SLEEP Mode**
Syntax:	SLEEP
Operands:	None
Operation:	0x00 → WDT; 0x00 → WDT pre-scaler; 1 → $\overline{TO}$; 0 → $\overline{PD}$
Status Affected:	$\overline{TO}$, $\overline{PD}$
Description:	Time-out status bit ($\overline{TO}$) is set. The power-down status bit ($\overline{PD}$) is cleared. The WDT is cleared. The processor is put into SLEEP mode.
Cycles:	1

SBCAR	**Subtract ACC from R with Carry**
Syntax:	SBCAR R, d
Operands:	0x00≤R≤0x3F d∈[0,1]
Operation:	R + $\overline{ACC}$ + C → dest
Status Affected:	C, DC, Z
Description:	Add the 2's complement data of the ACC register from register 'R' with Carry. If 'd' is 0 the result is stored in the ACC register. If 'd' is 1 the result is stored back in register 'R'.
Cycles:	1

SUBAR	**Subtract ACC from R**
Syntax:	SUBAR R, d
Operands:	0x00≤R≤0x3F d∈[0,1]
Operation:	R - ACC → dest
Status Affected:	C, DC, Z
Description:	Subtract (2's complement method) the ACC register from register 'R'. If 'd' is 0 the result is stored in the ACC register. If 'd' is 1 the result is stored back in register 'R'.
Cycles:	1

SUBIA	**Subtract ACC from Immediate**
Syntax:	SUBIA I
Operands:	0x00≤I≤0xFF
Operation:	I - ACC → ACC
Status Affected:	C, DC, Z
Description:	Subtract (2's complement method) the ACC register from the 8-bit immediate 'I'. The result is placed in the ACC register.
Cycles:	1

SWAPR	**Swap nibbles in R**
Syntax:	SWAPR R, d
Operands:	0x00≤R≤0x3F d∈[0,1]
Operation:	R<3:0> → dest<7:4>; R<7:4> → dest<3:0>
Status Affected:	None
Description:	The upper and lower nibbles of register 'R' are exchanged. If 'd' is 0 the result is placed in ACC register. If 'd' is 1 the result in placed in register 'R'.
Cycles:	1

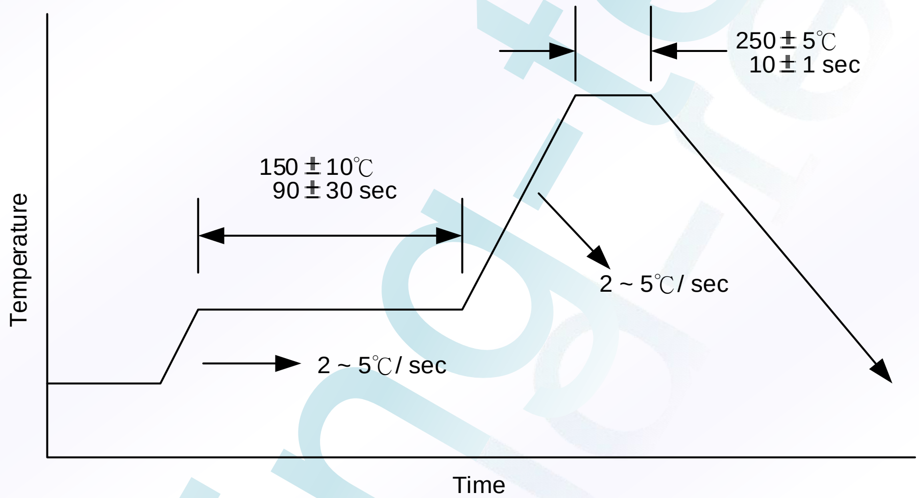
XORAR	Exclusive OR ACC with R
Syntax:	XORAR R, d
Operands:	0x00≤R≤0x3F d∈[0,1]
Operation:	ACC xor R → dest
Status Affected:	Z
Description:	Exclusive OR the contents of the ACC register with register 'R'. If 'd' is 0 the result is stored in the ACC register. If 'd' is 1 the result is stored back in register 'R'.
Cycles:	1

XORIA	Exclusive OR Immediate with ACC
Syntax:	XORIA I
Operands:	0x00≤I≤0xFF
Operation:	ACC xor I → ACC
Status Affected:	Z
Description:	The contents of the ACC register are XOR'ed with the 8-bit immediate 'I'. The result is placed in the ACC register.
Cycles:	1

4.0 ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
	Ambient Operating Temperature	-	0	-	70	°C
	Store Temperature	-	-65	-	150	°C
V_{DD}	DC Supply Voltage	-	0	-	6.0	V
	Input Voltage with respect to Ground	-	-0.3	-	V_{DD}+0.3	V
	ESD Susceptibility	HBM (Human Body Mode)	-	2.0	-	KV
		MM (Machine Mode)	-	200	-	V
	Lead Temperature	Soldering, 10 Sec	-	-	250	°C

4.1 PACKAGE IR Re-flow Soldering Curve



5.0 RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	DC Supply Voltage	-	2.0	-	5.5	V
	Operating Temperature	-	0	-	70	°C

6.0 ELECTRICAL CHARACTERISTICS

6.1 AC Characteristics

Ta=25°C

Symbol	Description	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
F_{HF}	HF Oscillation range	3V	HF mode	4	-	20	M_{HZ}
		5V		4	-	20	
F_{XT}	XT Oscillation range	3V	XT mode	0.455	-	20	M_{HZ}
		5V		0.455	-	20	
F_{LF}	LF oscillation range	3V	LF mode	32	-	32	K_{HZ}
		5V		32	-	32	
F_{ERC}	ERC Oscillation range	3V	ERC mode	DC	-	10	M_{HZ}
		5V		DC	-	18	
F_{ERIC}	ERIC Oscillation range	3V	ERIC mode	DC	-	8	M_{HZ}
		5V		DC	-	16	
F_{IRC}	Internal RC Oscillation range	3V	455K_{HZ} IRC mode	-3%	455	+3%	K_{HZ}
		5V		-3%	455	+3%	
		3V	1M_{HZ} IRC mode	-3%	1	+3%	M_{HZ}
		5V		-3%	1	+3%	
		3V	4M_{HZ} IRC mode	-3%	4	+3%	M_{HZ}
		5V		-3%	4	+3%	
		3V	8M_{HZ} IRC mode	-3%	8	+3%	M_{HZ}
		5V		-3%	8	+3%	
T_{WDT}	WDT period time	3V	WDT=4.5mS,	-	5.72	-	mS
		5V	Pre-scaler rate=1:1	-	4.36	-	
		3V	WDT=18mS,	-	23.08	-	
		5V	Pre-scaler rate=1:1	-	17.6	-	
		3V	WDT=72mS,	-	92.9	-	
		5V	Pre-scaler rate=1:1	-	70.54	-	
		3V	WDT=288mS,	-	368.37	-	
		5V	Pre-scaler rate=1:1	-	280.78	-	

Note: 1. In the ERIC mode, to maintain the accuracy of the internal RC oscillator frequency, a 300pF ~ 0.1uF decoupling capacitor should be connected between OSCI and V_{SS} and located as close to the device as possible.

2. At any time, a 0.1μF decoupling capacitor should be connected between V_{DD} and V_{SS} and device as close as possible.

6.2 DC Characteristics

Ta=25°C

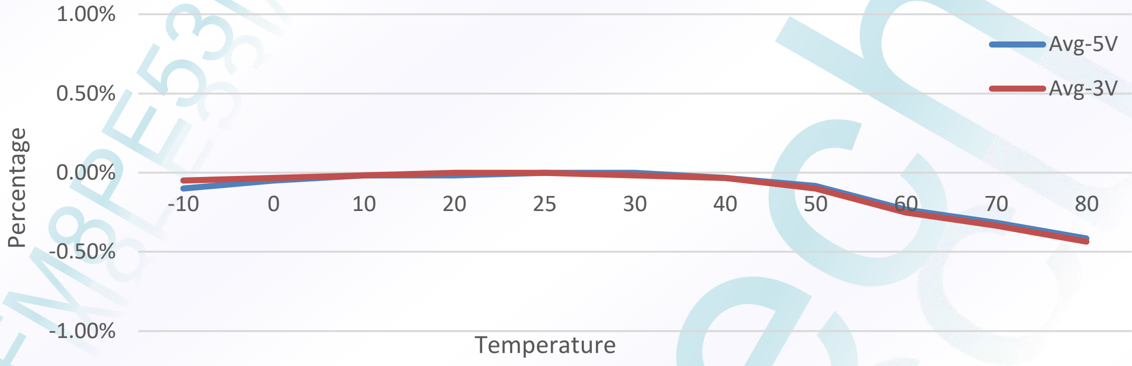
Under Operating Conditions, at two clock instruction cycles and WDT & LVDT are disable, I/O output float.

Symbol	Description	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{IH1}	Input high voltage, I/O Ports	3V	With Schmitt-trigger	-	1.41	V_{DD}	V
		5V		2.2	-	V_{DD}	
	Input high voltage, RSTB, T0CKI Pins	3V	With Schmitt-trigger	-	1.36	V_{DD}	
		5V		-	1.98	V_{DD}	
V_{IH2}	Input high voltage, I/O Ports	3V	Without Schmitt-trigger	-	1.26	V_{DD}	V
		5V		-	1.74	V_{DD}	
	Input high voltage, RSTB, T0CKI Pins	3V	Without Schmitt-trigger	-	1.2	V_{DD}	
		5V		-	1.69	V_{DD}	

Symbol	Description	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{IL1}	Input low voltage with Schmitt-trigger, I/O Ports	3V	With Schmitt-trigger	V_{SS}	0.98	-	V
		5V		V_{SS}	-	0.9	
	Input low voltage, RSTB, T0CKI Pins	3V	With Schmitt-trigger	V_{SS}	0.96	-	
		5V		V_{SS}	1.21	-	
V_{IL2}	Input low voltage, I/O Ports	3V	Without Schmitt-trigger	V_{SS}	1.12	-	V
		5V		V_{SS}	1.51	-	
	Input low voltage, RSTB, T0CKI Pins	3V	Without Schmitt-trigger	V_{SS}	1.12	-	
		5V		V_{SS}	1.56	-	
V_{LVDT}	LVDT voltage	-	LVDT=3.6V	3.06	3.6	4.14	V
		-	LVDT=2.6V	2.21	2.6	2.99	
		-	LVDT=2.4V	2.04	2.4	2.76	
		-	LVDT=2.2V	1.87	2.2	2.53	
		-	LVDT=2.0V	1.7	2.0	2.3	
		-	LVDT=1.8V	1.6	1.8	2.07	
I_{OH}	I/O Ports Drive current	3V	V_{OH}=0.9V_{DD}	-	1.67	-	mA
		5V		1.5	4.37	-	
I_{OL}	I/O Ports Sink current (Without IOB3 Pin)	3V	V_{OL}=0.1V_{DD}	-	9.46	-	mA
		5V		10	23.17	-	
	IOB3 Pin Sink current	3V	V_{OL}=0.1V_{DD}	-	9.33	-	
		5V		-	22.79	-	
I_{PH}	I/O Ports Pull-high current	3V	Input pin at V_{SS}	-	22.69	-	uA
		5V		63	74.07	93	
I_{PL}	Pull-low current	3V	Input pin at V_{DD}	-	12.58	-	uA
		5V		30	42.24	60	
I_{LVDT}	LVDT current	5V	LVDT=3.6V	-	1.13	-	uA
		3V	LVDT=2.6V	-	0.42	-	
		5V		-	1.42	-	
		3V	LVDT=2.4V	-	0.46	-	
		5V		-	1.53	-	
		3V	LVDT=2.2V	-	0.49	-	
		5V		-	1.68	-	
		3V	LVDT=2.0V	-	0.52	-	
		5V		-	1.76	-	
		3V	LVDT=1.8V	-	0.58	-	
		5V		-	1.92	-	
I_{WDT}	WDT current	3V	Sleep mode, Pre-scaler rate=1:256	-	0.53	-	uA
		5V		1	3.67	7	
I_{SB}	Sleep mode (Power down) current	3V	-	-	<1	-	uA
		5V		-	<1	1	
I_{DD1}	Operating current	3V	IRC 8M_{HZ}, 2T	-	0.6	-	mA
		5V		-	1.15	-	
I_{DD2}	Operating current	3V	IRC 4M_{HZ}, 2T	-	0.33	-	mA
		5V		-	0.63	-	
I_{DD3}	Operating current	3V	IRC 1M_{HZ}, 2T	-	0.12	-	mA
		5V		-	0.25	-	
I_{DD4}	Operating current	3V	IRC 455K_{HZ}, 2T	-	0.08	-	mA
		5V		-	0.19	-	

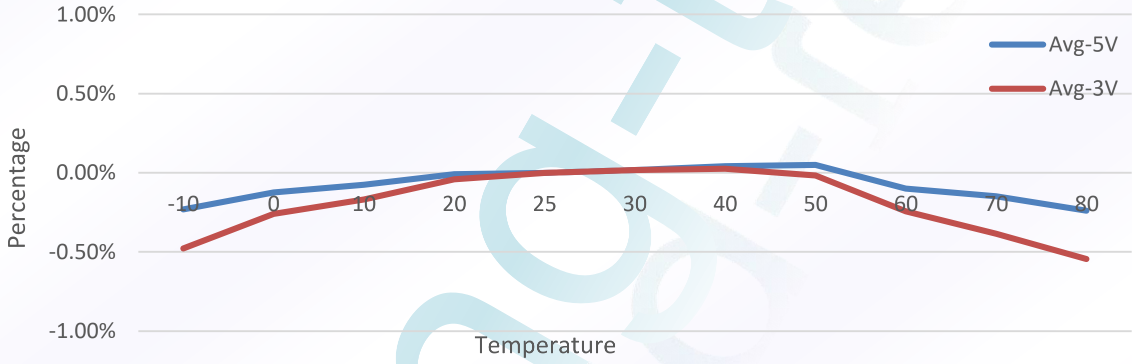
6.3 ELECTRICAL CHARACTERISTICS Typical charts of FM8PE56M

6.3.1 IRC 4MHZ vs. Temperature



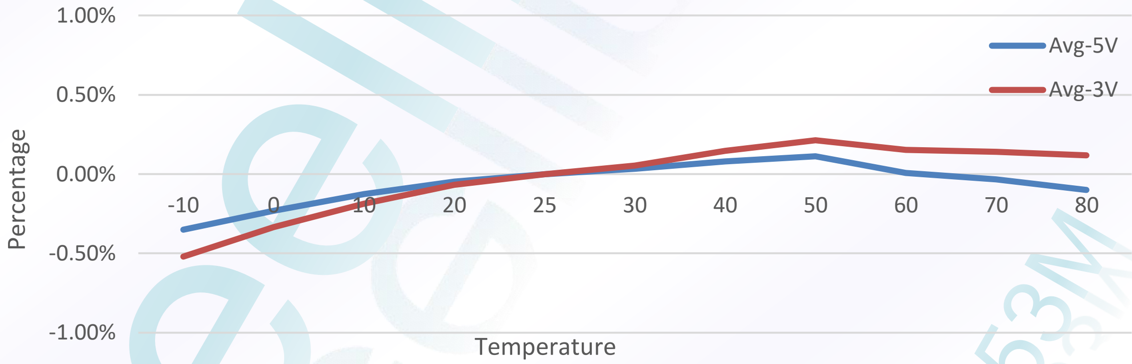
Note: Curves are for design reference only.

6.3.2 IRC 8MHZ vs. Temperature



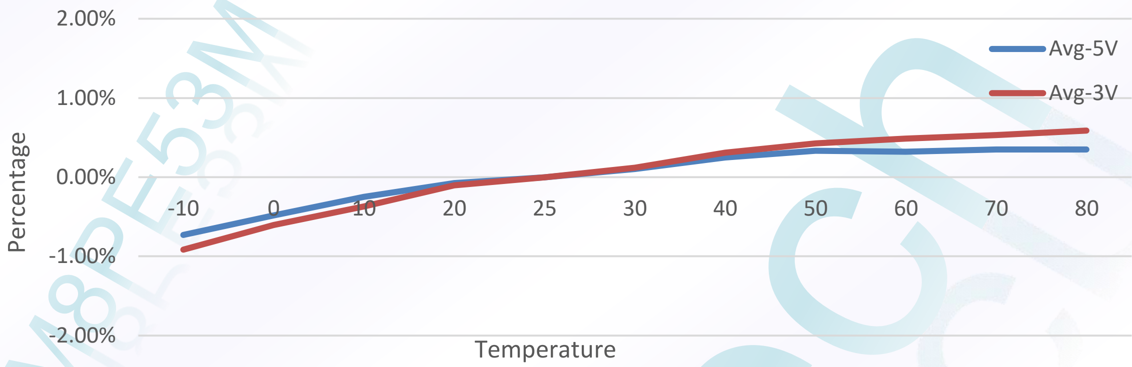
Note: Curves are for design reference only.

6.3.3 IRC 1MHZ vs. Temperature



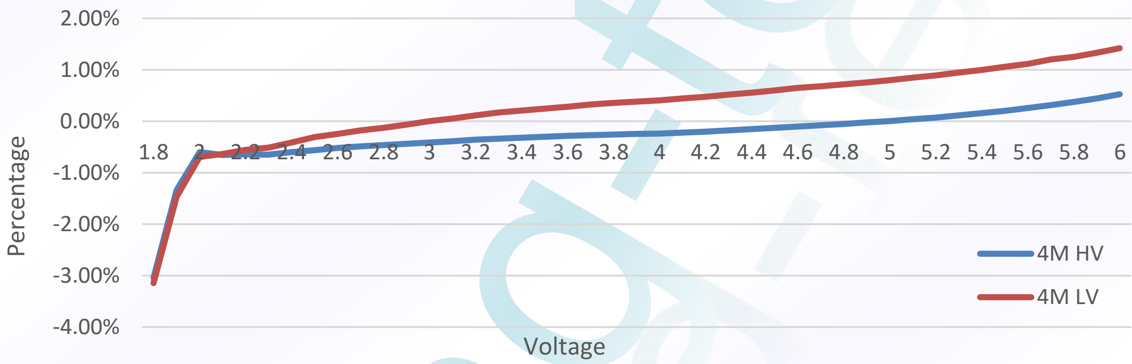
Note: Curves are for design reference only.

6.3.4 IRC 455KHZ vs. Temperature



Note: Curves are for design reference only.

6.3.5 IRC 4 MHZ vs. Supply Voltage (Ta=25°C)

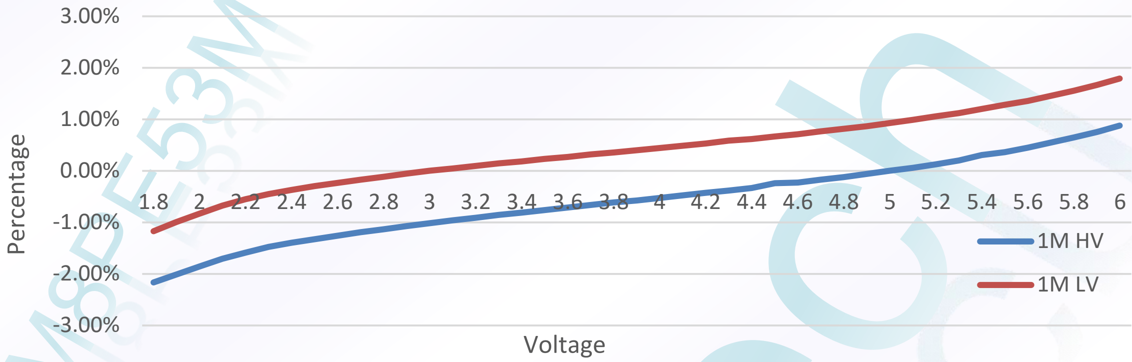


Note: Curves are for design reference only.

6.3.6 IRC 8 MHZ vs. Supply Voltage (Ta=25°C)

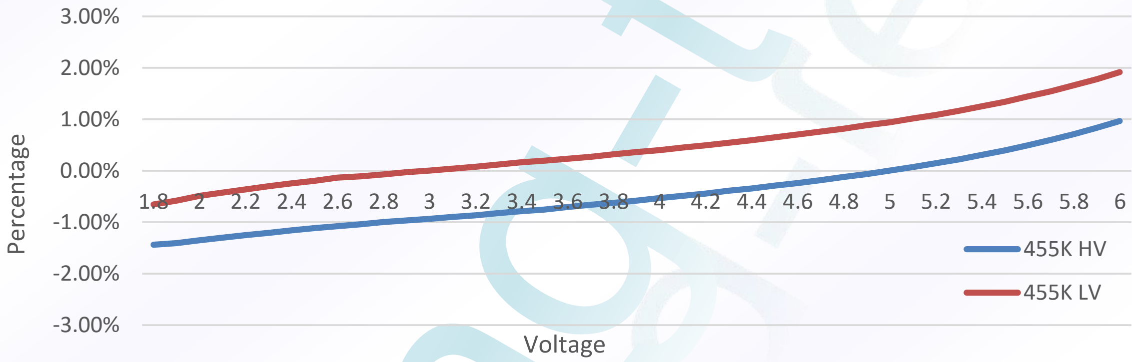
Note: Curves are for design reference only.

6.3.7 IRC 1 MHZ vs. Supply Voltage (Ta=25°C)



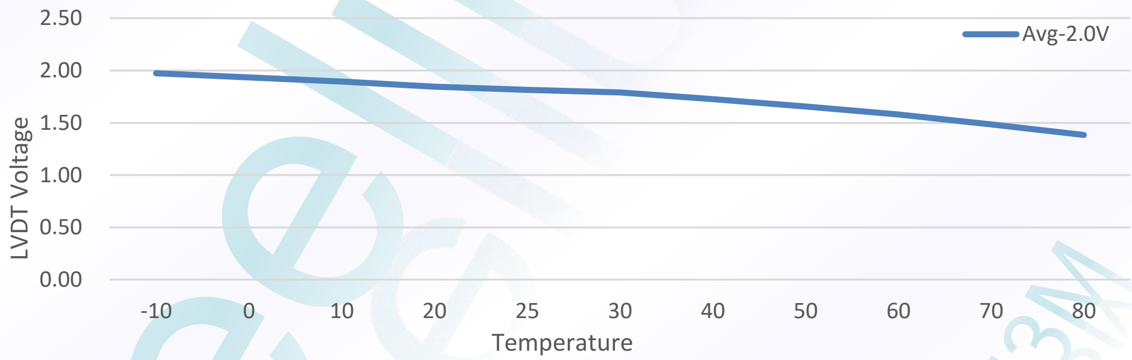
Note: Curves are for design reference only.

6.3.8 IRC 455 KHZ vs. Supply Voltage (Ta=25°C)



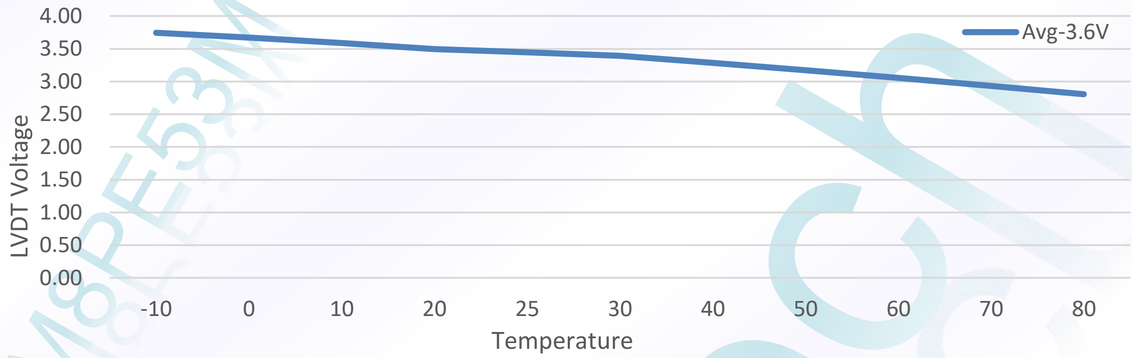
Note: Curves are for design reference only.

6.3.9 Low Voltage Detect (LVDT=2.0V) vs. Temperature



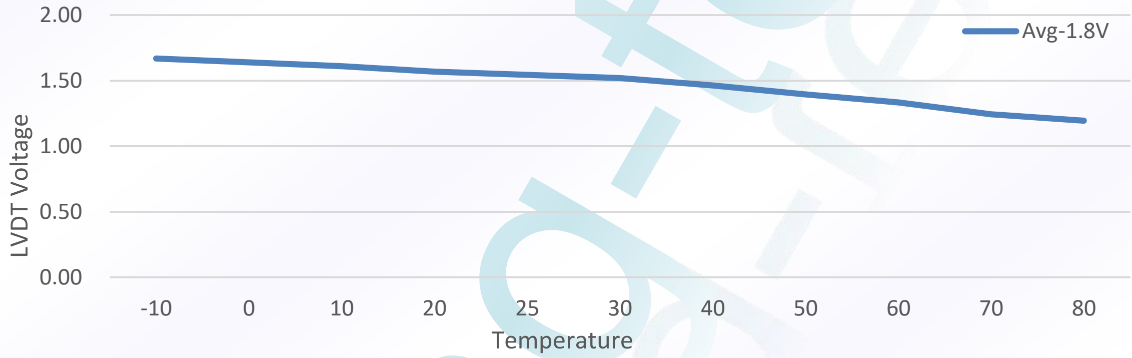
Note: Curves are for design reference only.

6.3.10 Low Voltage Detect (LVDT=3.6V) vs. Temperature



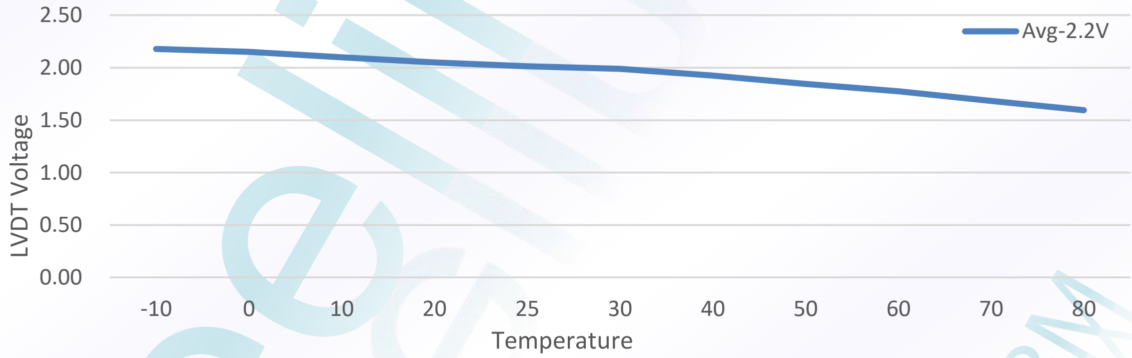
Note: Curves are for design reference only.

6.3.11 Low Voltage Detect (LVDT=1.8V) vs. Temperature



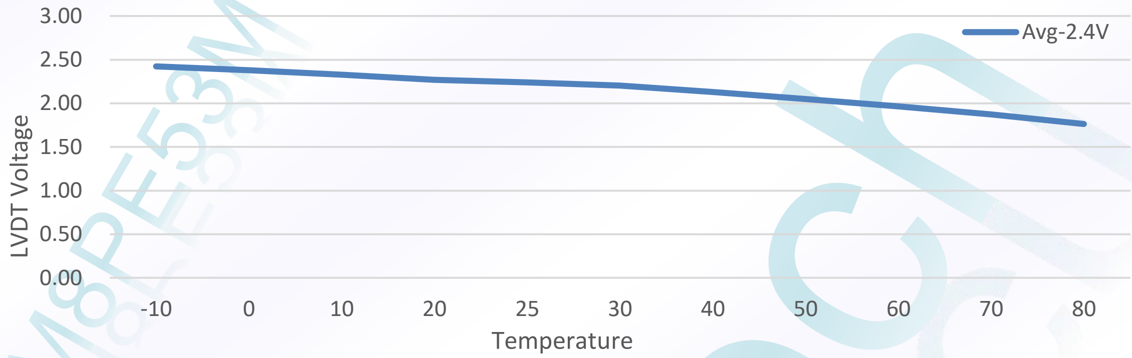
Note: Curves are for design reference only.

6.3.12 Low Voltage Detect (LVDT=2.2V) vs. Temperature



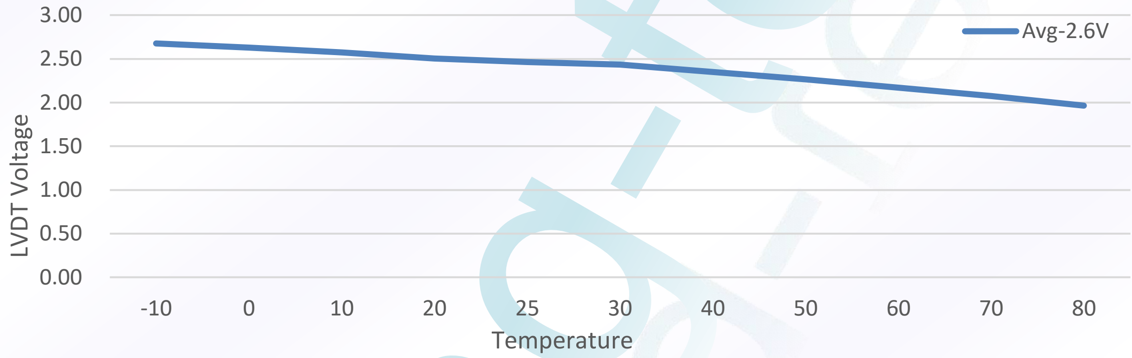
Note: Curves are for design reference only.

6.3.13 Low Voltage Detect (LVDT=2.4V) vs. Temperature



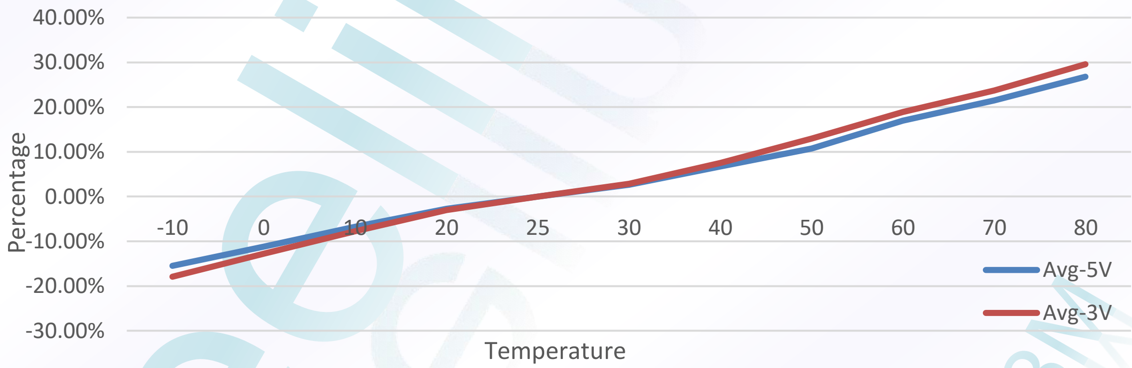
Note: Curves are for design reference only.

6.3.14 Low Voltage Detect (LVDT=2.6V) vs. Temperature



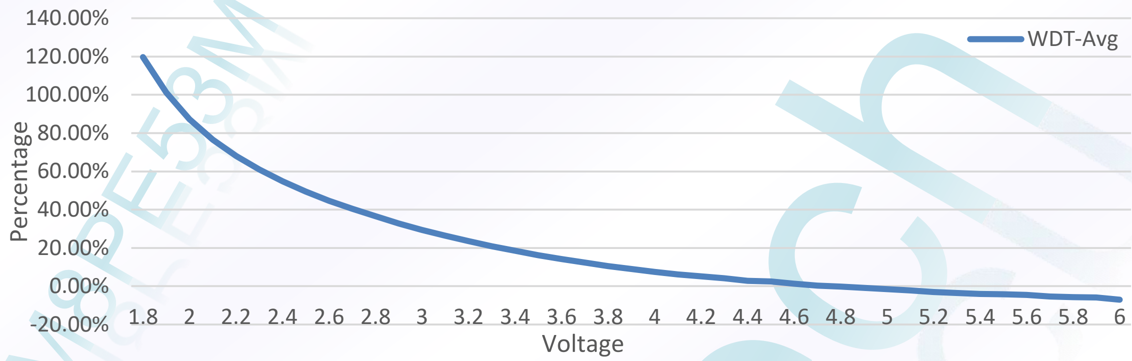
Note: Curves are for design reference only.

6.3.15 WDT 4.5mS, 18mS, 72mS and 288mS Reset time vs. Temperature



Note: Curves are for design reference only.

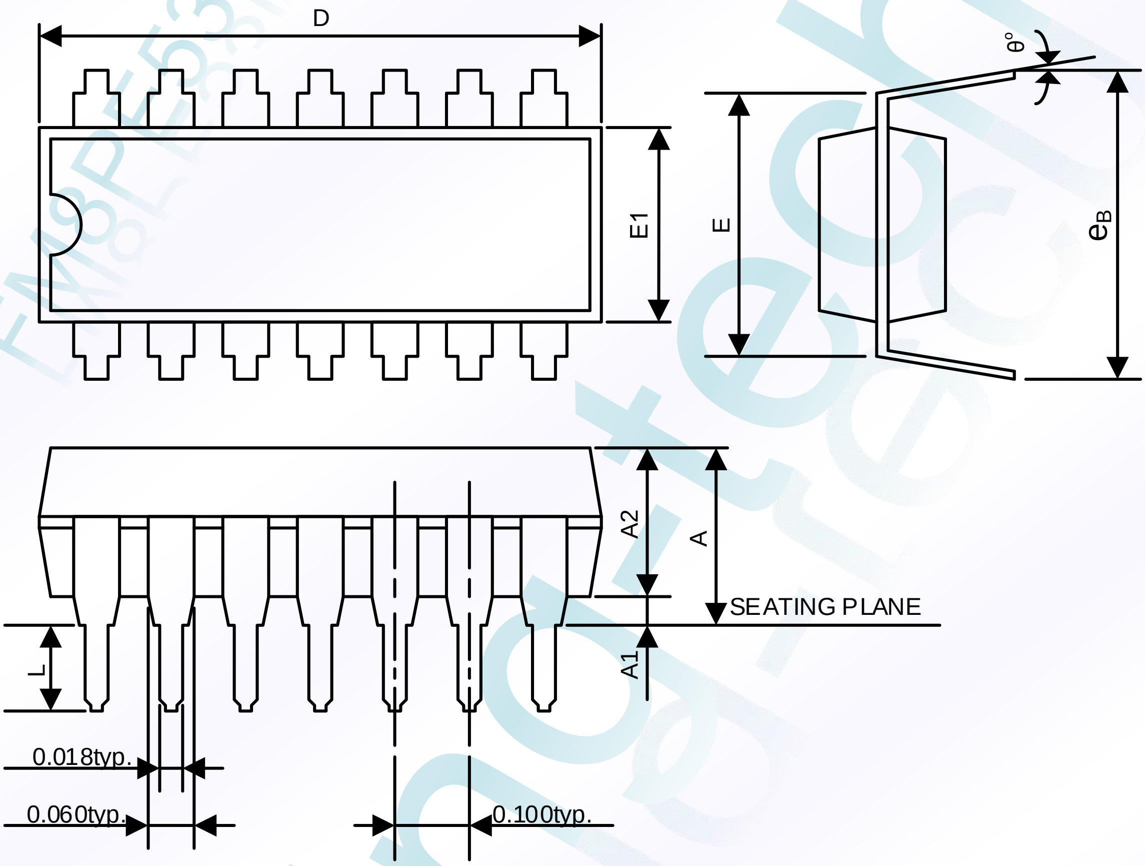
6.3.16 WDT 4.5mS, 18mS, 72mS and 288mS Reset time vs. Supply Voltage (Ta=25°C)



Note: Curves are for design reference only.

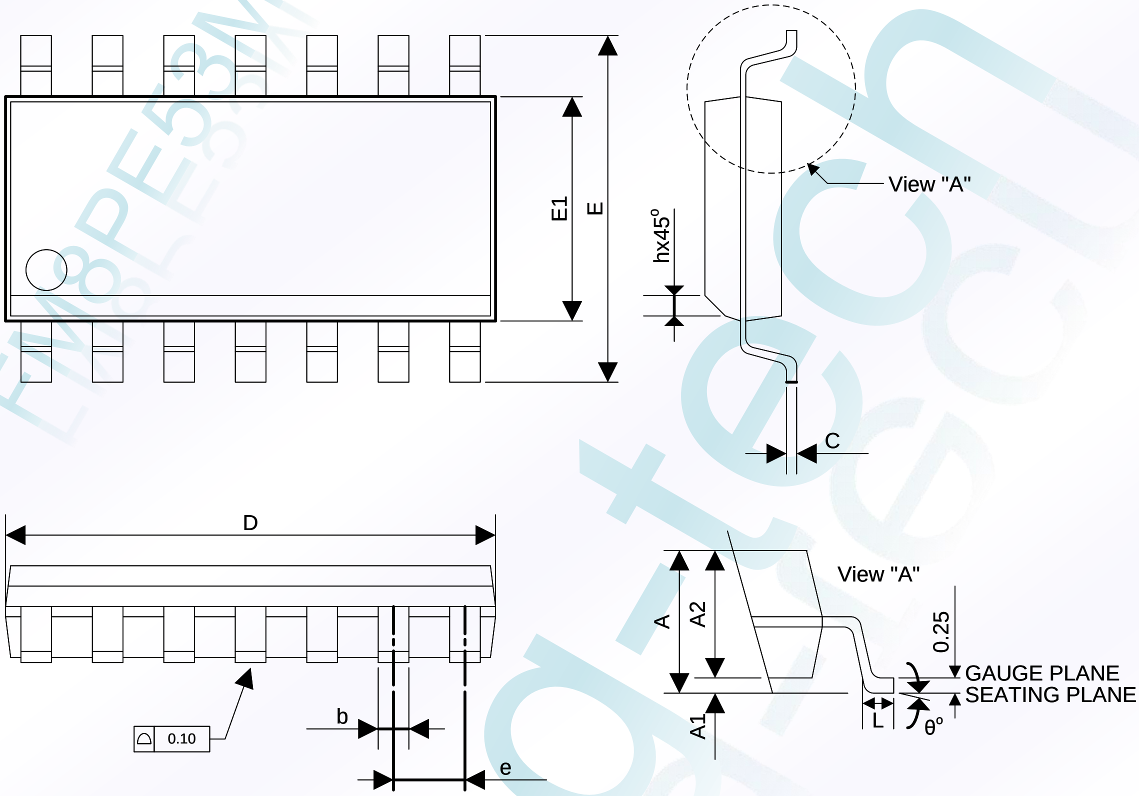
7.0 PACKAGE DIMENSION

7.1 14-PIN PDIP



Symbols	Dimension In Inches		
	Min	Nom	Max
A	-	-	0.210
A1	0.015	-	-
A2	0.125	0.130	0.135
D	0.735	0.750	0.775
E	0.300 BSC.		
E1	0.245	0.250	0.255
L	0.115	0.130	0.150
eB	0.335	0.355	0.375
θ°	0°	7°	15°

7.2 14-PIN SOP 150mil



Symbols	Dimension In MM		
	Min	Nom	Max
A	-	-	1.75
A1	0.10	-	0.25
A2	1.25	-	-
b	0.31	-	0.51
C	0.10	-	0.25
D	8.65BSC		
E	6.00BSC		
E1	3.90BSC		
e	1.27BSC		
L	0.40	-	1.27
H	0.25		0.50
θ	0°	-	8°

8.0 ORDERING INFORMATION

OTP Type MCU	Package Type	Pin Count	Package Size	MOQ	MSL	Sample Stock
FM8PE53MP	PDIP	14	300mil	3,000EA/Tube	3	Available
FM8PE53MD	SOP	14	150mil	3,000EA/Tube 3,000EA/Reel	3	Available