FEELING TECHNOLOGY

FM8PE531M

OTP-Based 8-Bit Microcontroller

Devices Included in this Data Sheet:

- FM8PE531MA: 14-pin OTP device
- FM8PE531MB: 16-pin OTP device

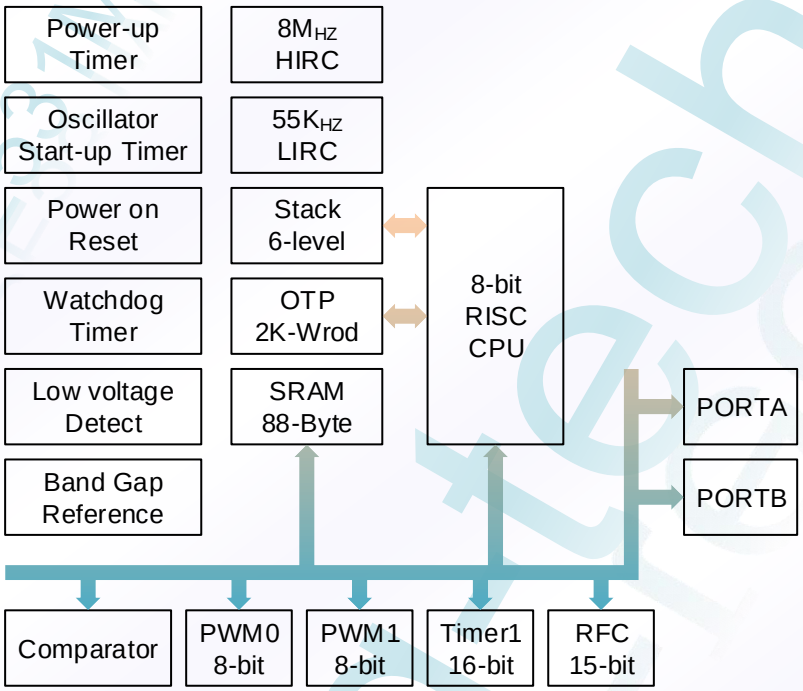
GENERAL DESCRIPTION

The FM8PE531M is a low-cost, high speed, OTP-based 8-bit CMOS microcontrollers. It employs a RISC architecture with only 37 instructions. All instructions are single cycle except for program branches which take two cycles. The easy to use and easy to remember instruction set reduces development time significantly.
The FM8PE531M consists of Power-on Reset (POR), Brown-out Reset (BOR), Power-up Reset Timer (PWRT), Watchdog Timer, OTP, SRAM, tristate I/O port, I/O pull-high control, Power saving SLEEP mode, real time programmable clock/counter, Interrupt, PWM, Comparator (with CV_{REF}, Fixed Band Gap reference voltage), Wake-up from SLEEP mode products.

FEATURES

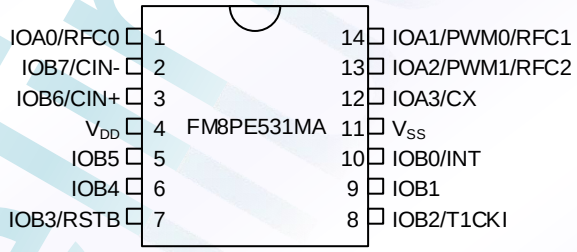
- 2K Word on chip OTP-ROM and 88 Bytes on chip general purpose registers (SRAM).
- 6-level deep hardware stack.
- One analog comparator.
  - Internal reference voltage: 16-step CV_{REF} module, 1.2V fixed voltage reference.
- One 16-bit real timer/Counter with 2-bit programmable pre-scaler.
- Two 8-bit fixed period-cycle PWM.
- Three channel 15-bit RFC.
- Six levels LVDT (Low Voltage Detect): 3.6V, 2.6V, 2.4V, 2.2V, 2.0V and 1.8V.
- Power-up Reset Timer (PWRT)
- On chip Watchdog Timer (WDT) with internal oscillator for reliable operation.
- Two I/O port, PORTA and PORTB with independent direction control:
  - 13 Bi-direction I/O pin (Programmable Pull-up enable in Input mode).
  - One Input /Open-drain pin (IOB3/RSTB).
- Two kinds of interrupt source:
  - 4 internal interrupt sources: Timer1, RFC, Comparator and LVDT.
  - 1 external interrupt sources: INT pin.
- Wake-up from SLEEP:
  - ALL pin (IOA5~IOA0, IOB7~IOB0) input change wake-up.
  - WDT overflow.
- Power saving SLEEP mode.
- Selectable oscillator options:
  -HIRC: Internal Resistor/Capacitor 8M_{HZ} Oscillator.
  -LIRC: Internal Resistor/Capacitor 55K_{HZ} Oscillator.
- Wide-operating voltage range: 2.0V to 5.5V.

BLOCK DIAGRAM



PIN CONNECTION

DIP/SOP14



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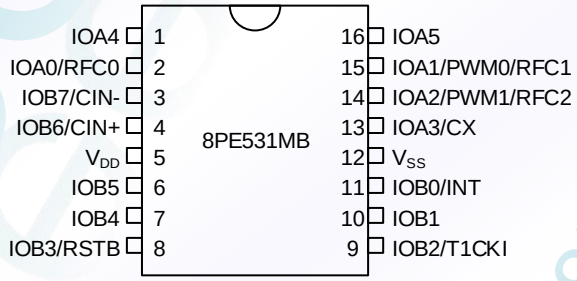


PIN DESCRIPTIONS

Name	I/O	Description
IOA0/RFC0	I/O	• Bi-direction I/O port with wake-up function (programmable Pull-high in Input mode). • The RC oscillator network output0 of RFC module.
IOA1/PWM0/RFC1	I/O	• Bi-direction I/O port with wake-up function (programmable Pull-high in Input mode). • PWM0 output. • The RC oscillator network output1 of RFC module.
IOA2/PWM1/RFC2	I/O	• Bi-direction I/O port with wake-up function (programmable Pull-high in Input mode). • PWM1 output. • The RC oscillator network output2 of RFC module.
IOA3/CX	I/O	• Bi-direction I/O port with wake-up function (programmable Pull-high in Input mode). • The RC oscillator network input of RFC module.
IOA4, IOA5 IOB1, IOB4, IOB5	I/O	• Bi-direction I/O port with wake-up function (programmable Pull-high in Input mode).
IOB0/INT	I/O	• Bi-direction I/O port with wake-up function (programmable Pull-high in Input mode). • External interrupt input.
IOB2/T1CKI	I/O	• Bi-direction I/O port with wake-up function (programmable Pull-high in Input mode). • External clock input to Timer1.
IOB3/RSTB	I/O	• Input pin only with system wake-up/pin change interrupt function; **voltage on this pin must not exceed V_{DD}.** • System clear (RESET) input. This pin is an active low RESET to the device. • Open-Drain output.
IOB6/CIN+	I/O	• Bi-direction I/O port with wake-up function (programmable Pull-high in Input mode). • Comparator positive input.
IOB7/CIN-	I/O	• Bi-direction I/O port with wake-up function (programmable Pull-high in Input mode). • Comparator negative input.
V_{DD}	-	Positive supply.
V_{SS}	-	Ground.

Legend: I=input, O=output, I/O=input/output.

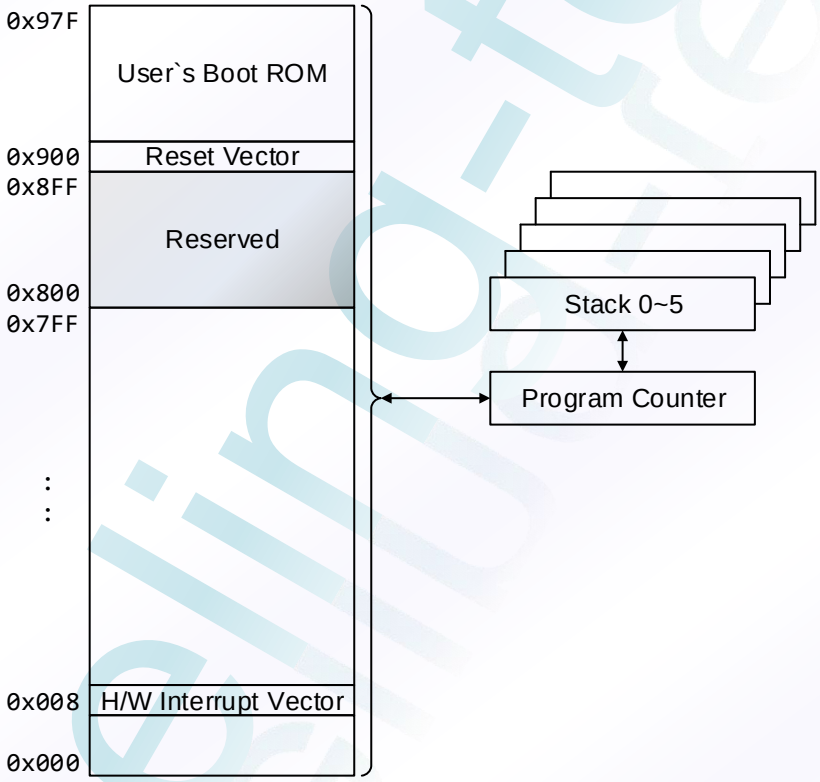
1.0 MEMORY ORGANIZATION

FM8PE531M memory is organized into program memory and data memory.

1.1 Program Memory Organization

The FM8PE531M have a 12-bit Program Counter capable of addressing a 2K program memory space.
The RESET vector for the FM8PE531M is at 0x900.
The H/W interrupt vector is at 0x008.
CALL and GOTO instructions only have a 10-bit address range. This 10-bit address range allows a branch within a 1K program memory page size. To allow CALL and GOTO instructions to address the entire 2K program memory address range for 8PE531M, there is other two bits to specify the program memory page. This paging bit comes from the PG<1:0> bits (STATUS<6:5>, STATUS<6> must keep 0.).

Figure 1.1: Program Memory Map and STACK



1.2 Data Memory Organization

Data memory is composed of Special Function Registers and General Purpose Registers.
The General Purpose Registers are accessed either directly or indirectly through the FSR register.
The Special Function Registers are registers used by the CPU and peripheral functions to control the operation of the device.
In FM8PE531M, the data memory is partitioned into four banks. Switching between these banks requires the RP1, RP0 bits in the FSR register to be configured for the desired bank.

Table 1.1: Registers File Map for FM8PE531M

FSR<7:6> / Address	Description			
	0 0 Bank 0	0 1 Bank 1	1 0 Bank 2	1 1 Bank 3
0x00	INDF			
0x02	PCL			
0x03	STATUS			
0x04	FSR			
0x05	IOSTA			
0x06	PORTA			
0x07	IOSTB			
0x08	PORTB			
0x09	T1CON			
0x0A	TMR1LB			
0x0B	TMR1HB			
0x0C	OSCCON			
0x0D	LVDTCON			
0x0E	INTEN			
0x0F	INTFLAG			
0x10	PWMCON		AWUCON	
0x11	P0DPR		APHCON	
0x12	P1DPR		BWUCON	
0x13	RFCCON		BPHCON	
0x14	RFCDLB		CMPCON1	
0x15	RFCDHB		CMPCON2	
0x16	PCHBUF			
0x18 | 0x2F	General Purpose Registers	Memory back to address in Bank 0		
0x30 | 0x3F	General Purpose Registers	General Purpose Registers	General Purpose Registers	General Purpose Registers

Table 1.2: Operational Registers Map

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
Unbanked									
0x00 (r/w)	INDF	Uses contents of FSR to address data memory (not a physical register)							
0x02 (r/w)	PCL	Low order 8 bits of PC							
0x03 (r/w)	STATUS	RST	PG1	PG0	$\overline{TO}$	$\overline{PD}$	Z	DC	C
0x04 (r/w)	FSR	RP1	RP0	Indirect data memory address pointer					
0x05 (r/w)	IOSTA	-	-	IOSTA5	IOSTA4	IOSTA3	IOSTA2	IOSTA1	IOSTA0
0x06 (r/w)	PORTA	-	-	IOA5	IOA4	IOA3	IOA2	IOA1	IOA0
0x07 (r/w)	IOSTB	IOSTB7	IOSTB6	IOSTB5	IOSTB4	IOSTB3	IOSTB2	IOSTB1	IOSTB0
0x08 (r/w)	PORTB	IOB7	IOB6	IOB5	IOB4	IOB3	IOB2	IOB1	IOB0
0x09 (r/w)	T1CON	-	-	-	T1PS1	T1PS0	GP	T1CS	T1EN
0x0A (r/w)	TMR1LB	Low byte of 16-bit real-time clock/counter 1							
0x0B (r/w)	TMR1HB	High byte of 16-bit real-time clock/counter 1							
0x0C (r/w)	OSCCON	WDTEN	IRCEN	WDTSEL1	WDTSEL0	CPUS	IRCF2	IRCF1	IRCF0
0x0D (r/w)	LVDTCON	EIS	RDPORT	IOB3EN	LVREN	INTEDG	LVDSEL2	LVDSEL1	LVDSEL0
0x0E (r/w)	INTEN	GIE	-	-	LVDTIE	CMPIE	INTIE	RFCIE	T1IE
0x0F (r/w)	INTFLAG	-	-	-	LVDTIF	CMPIF	INTIF	RFCIF	T1IF
0x16 (w)	PCHBUF	-	-	-	-	-	-	2 MSBs Buffer of PC	
Bank0, 1									
0x10 (r/w)	PWMCON	-	-	-	PWMCS2	PWMCS1	PWMCS0	P1EN	P0EN
0x11 (r/w)	P0DPR	PWM0 Duty Compare Pre-set register							
0x12 (r/w)	P1DPR	PWM1 Duty Compare Pre-set register							
0x13 (r/w)	RFCCON	RFCON	START	-	RFCMOD	-	-	RFCS1	RFCS0
0x14 (r)	RFCDLB	Low byte of 15 bit RFC conversion result							
0x15 (r)	RFCDHB	RFCOV	RFCD14	RFCD13	RFCD12	RFCD11	RFCD10	RFCD9	RFCD8
Bank2, 3									
0x10 (r/w)	AWUCON	-	-	WUA5	WUA4	WUA3	WUA2	WUA1	WUA0
0x11 (r/w)	APHCON	-	-	/PHA5	/PHA4	/PHA3	/PHA2	/PHA1	/PHA0
0x12 (r/w)	BWUCON	WUB7	WUB6	WUB5	WUB4	WUB3	WUB2	WUB1	WUB0
0x13 (r/w)	BPHCON	/PHB7	/PHB6	/PHB5	/PHB4	GP	/PHB2	/PHB1	/PHB0
0x14 (r/w)	CMPCON1	-	-	COUT	CINV	CINS	CM2	CM1	CM0
0x15 (r/w)	CMPCON2	-	-	CVREN	CVRR	CVR3	CVR2	CVR1	CVR0

Legend: - = unimplemented, read as '0'.

2.0 FUNCTIONAL DESCRIPTIONS

2.1 Operational Registers

2.1.1 INDF (Indirect Addressing Register)

Read/Write-POR		R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x00	INDF	Uses contents of FSR to address data memory (not a physical register)							

Legend: x = unknown, more bits' default state, please refer to Table 2.3.

The INDF Register is not a physical register. Any instruction accessing the INDF register can actually access the register pointed by FSR Register. Reading the INDF register itself indirectly (FSR="0x00") will read 0x00. Writing to the INDF register indirectly results in a no-operation (although status bits may be affected).

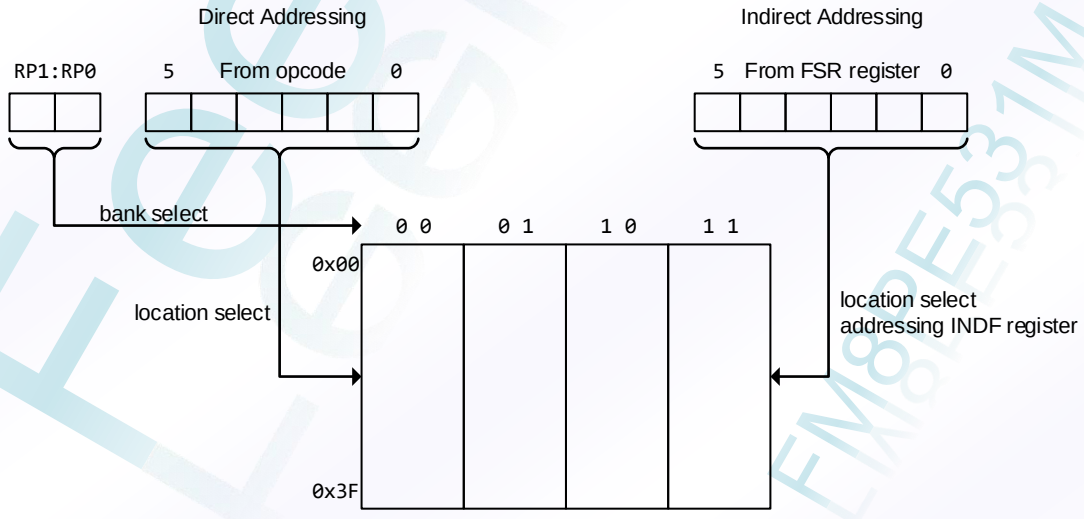
The bits 5-0 of FSR register are used to select up to 64 registers (address 0x00 ~ 0x3F).
In FM8PE531M, the data memory is partitioned into four banks. Switching between these banks requires the RP1 and RP0 bits in the FSR register to configure for the desired bank. The lower locations of each bank are reserved for the Special Function Registers. Above the Special Function Registers are General Purpose Registers. Some Special Function Registers and some of General Purpose Registers from other banks are mirrored in bank 0 for code reduction and quicker access.

RP1:RP0		Accessed Bank
0	0	0
0	1	1
1	0	2
1	1	3

Example 2.1: INDIRECT ADDRESSING

- Register file 0x18 contains the value 0x10
- Register file 0x19 contains the value 0x0A
- Load the value 0x18 into the FSR Register
- A read of the INDF Register will return the value of 0x10
- Increment the value of the FSR Register by one (@FSR=0x19)
- A read of the INDF register now will return the value of 0x0A.

Figure 2.1: Direct/Indirect Addressing



2.1.2 PCL (Low Byte of Program Counter) & Stack

Read/Write-POR		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x02	PCL	Low order 8 bits of PC							

Note: more bits' default state, please refer to Table 2.3.

FM8PE531M devices have a 12-bit wide Program Counter (PC) and six-level deep 12-bit hardware push/pop stack. The low byte of PC is called the PCL register. This register is readable and writable. The high byte of PC is called the PCH register. This register contains the PC<11:8> bits and is not directly readable or writable. All updates to the PCH register go through the PCHBUF register and PG<1:0> bits (STATUS<6:5>). As a program instruction is executed, the Program Counter will contain the address of the next program instruction to be executed. The PC value is increased by one, every instruction cycle, unless an instruction changes the PC.

For a GOTO instruction, the PC<9:0> is provided by the GOTO instruction word. The PC<11:10> is updated from the PG<1:0> bits (STATUS<6:5>). The PCL register is mapped to PC<7:0>.

For a CALL instruction, the PC<9:0> is provided by the CALL instruction word. The PC<11:10> is updated from the PG<1:0> bits (STATUS<6:5>). The next PC will be loaded (PUSHed) into the top of STACK. The PCL register is mapped to PC<7:0>.

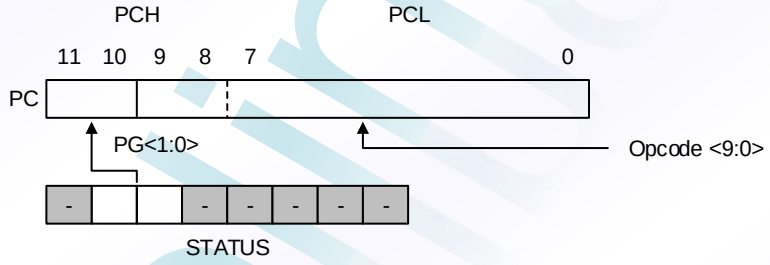
For a RETIA, RETFIE, or RETURN instruction, the PC are updated (POPed) from the top of STACK. The PCL register is mapped to PC<7:0>.

For any instruction where the PCL is the destination, the PC<7:0> is provided by the instruction word or ALU result; the PC<9:8> bits will be fixed loading as '0'. The PC<11:8> is updated from the PCHBUF<1:0>bits and PG<1:0> bits (STATUS<6:5>).

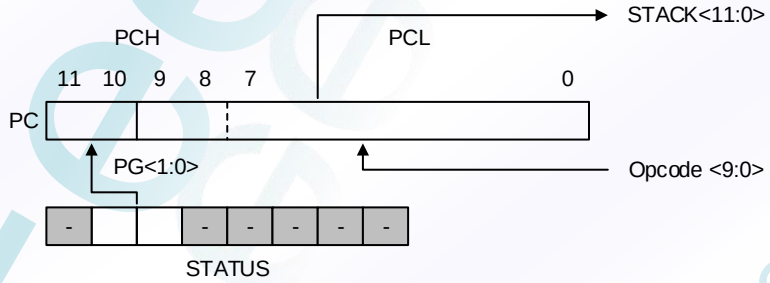
Please note: the PCHBUF is write-only register. If read, it will read as '0'.

Figure 2.2: Loading of PC in Different Situations

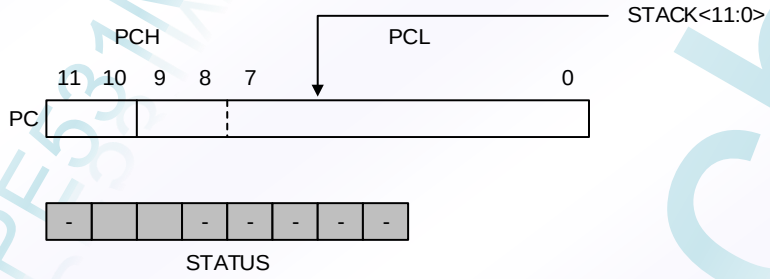
Situation 1: **GOTO** Instruction



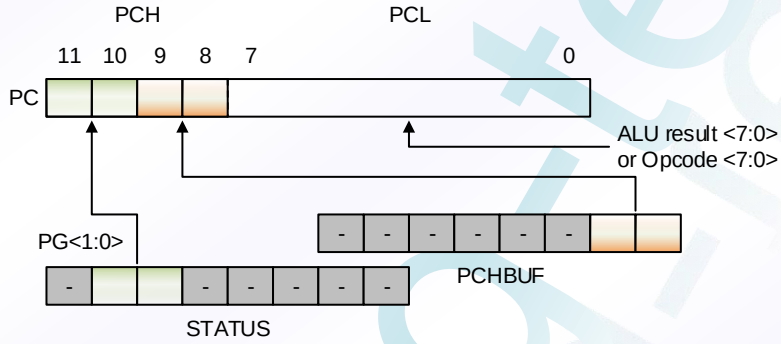
Situation 2: **CALL** Instruction



Situation 3: **RETIA**, **RETFIE**, or **RETURN** Instruction



Situation 4: Instruction with PCL as destination



2.1.3 STATUS (Status Register)

Read/Write-POR		R/W-0	R/W-1	R/W-0	R-#	R-#	R/W-x	R/W-x	R/W-x
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x03	STATUS	RST	PG1	PG0	$\overline{TO}$	$\overline{PD}$	Z	DC	C

Legend: x = unknown, # = refer Table 2.4 for detail description; more bits' default state, please refer to Table 2.3.

This register contains the arithmetic status of the ALU, the RESET status.
If the STATUS Register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS Register as destination may be different than intended. For example, CLRR STATUS will clear the upper three bits and set the Z bit. This leaves the STATUS Register as 000u u1uu (where u = unchanged).

C: Carry/borrow bit.
ADDAR, ADDIA, ADCAR
= 0, No Carry occurred.
= 1, Carry occurred.
SUBAR, SUBIA, SBCAR
= 0, Borrow occurred.
= 1, No borrow occurred.
Note: A subtraction is executed by adding the two's complement of the second operand. For rotate (RRR, RLR) instructions, this bit is loaded with either the high or low order bit of the source register.

DC: Half carry/half borrow bit.
ADDAR, ADDIA, ADCAR
= 0, No Carry from the 4th low order bit of the result occurred.
= 1, Carry from the 4th low order bit of the result occurred.
SUBAR, SUBIA, SBCAR
= 0, Borrow from the 4th low order bit of the result occurred.
= 1, No Borrow from the 4th low order bit of the result occurred.

Z: Zero bit.
= 0, The result of a logic operation is not zero.
= 1, The result of a logic operation is zero.

$\overline{PD}$: Power down flag bit.
= 0, by the SLEEP instruction.
= 1, after power-up or by the CLRWDT instruction.

$\overline{TO}$: Time overflow flag bit.
= 0, a watch-dog time overflow occurred.
= 1, after power-up or by the CLRWDT or SLEEP instruction.

PG1:PG0: Program memory page select bits. Used for GOTO, CALL, or any instruction with PCL as destination.

PG1:PG0		Program Memory Page [Address]
0	0	Page 0 [0x000~0x3FF]
0	1	Page 1 [0x400~0x7FF]
1	0	Page 2 [0x900~0x97F]
1	1	Inhibit

Note: Page0 and 1 is User's main program area, page2 is User's Boot ROM.

RST: Bit for wake-up type.
= 0, Wake-up from other reset types.
= 1, Wake-up from SLEEP.

2.1.4 FSR (Indirect Data Memory Address Pointer)

Read/Write-POR		R/W-0	R/W-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x04	FSR	RP1	RP0	Indirect data memory address pointer					

Note: more bits' default state, please refer to Table 2.3.

Bit5:Bit0: Select registers address in the indirect addressing mode. See section 2.1.1 for detail description.

RP1:RP0: These bits are used to switching the bank of four data memory banks. See section 2.1.1 for detail description.

2.1.5 IOSTA & IOSTB (Port I/O Control Register)

Read/Write-POR		-	-	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x05	IOSTA	-	-	IOSTA5	IOSTA4	IOSTA3	IOSTA2	IOSTA1	IOSTA0

Read/Write-POR		R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x07	IOSTB	IOSTB7	IOSTB6	IOSTB5	IOSTB4	IOSTB3	IOSTB2	IOSTB1	IOSTB0

Legend: - = unimplemented, read as '0'; more bits' default state, please refer to Table 2.3.

IOSTA5:IOSTA0: PORTA I/O control bit.
= 0, PORTA pin configured as an output.
= 1, PORTA pin configured as an input (tristate).

IOSTB7:IOSTB0: PORTB I/O control bit.
= 0, PORTB pin configured as an output.
= 1, PORTB pin configured as an input (tristate).
Note: IOB3 is open-drain output only if IOSTB3 = 0.

2.1.6 PORTA & PORTB (Port Data Register)

Read/Write-POR		-	-	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x06	PORTA	-	-	IOA5	IOA4	IOA3	IOA2	IOA1	IOA0

Read/Write-POR		R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x08	PORTB	IOB7	IOB6	IOB5	IOB4	IOB3	IOB2	IOB1	IOB0

Legend: - = unimplemented, read as '0', x = unknown, more bits' default state, please refer to Table 2.3.

Reading the port (PORTA and PORTB register) reads the status of the pins independent of the pin's input/output modes. Writing to these ports will write to the port data latch.

IOA5:IOA0:PORTA I/O pin.
= 0, Port pin is low level.
= 1, Port pin is high level.

IOB7:IOB0:PORTB I/O pin.
= 0, Port pin is low level.
= 1, Port pin is high level.
Note:1. IOB3 is open-drain output only if IOSTB3 = 0.
2. **Before setting IOB3 output 0, user must first IOB3EN bit set to 1, or they may cause reset.**

2.1.7 T1CON (Timer 1 Control Register)

Read/Write-POR		-	-	-	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x09	T1CON	-	-	-	T1PS1	T1PS0	GP	T1CS	T1EN

Legend: - = unimplemented, read as '0'; more bits' default state, please refer to Table 2.3.

T1EN: Timer1 Enable/Disable bit.
= 0, Disable Timer1.
= 1, Enable Timer1.

T1CS: Timer1 clock source select bit.
= 0, Internal instruction clock cycle.
= 1, External T1CKI pin.

GP: General purpose read/write bits.

T1PS1:T1PS0: Timer1 pre-scaler rate select bits.

T1PS1:T1PS0		Pre-scaler Rate
0	0	1:1
0	1	1:2
1	0	1:4
1	1	1:8

2.1.8 TMR1LB and TMR1HB (Timer 1 Clock/Counter Register)

Read/Write-POR		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x0A	TMR1LB	Low byte of 16-bit real-time clock/counter 1							

Read/Write-POR		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x0B	TMR1HB	High byte of 16-bit real-time clock/counter 1							

Note: more bits' default state, please refer to Table 2.3.

The Timer1 is a 16-bit timer/counter. The clock source of Timer1 can come from the instruction cycle clock or by an external clock source (T1CKI pin) defined by T1CS bit (T1CON<1>). If T1CKI pin is selected, the Timer1 is increased by T1CKI signal rising edge.

2.1.9 OSCCON (Oscillator Control Register)

Read/Write-POR		R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x0C	OSCCON	WDTEN	IRCEN	WDTSEL1	WDTSEL0	CPUS	IRCF2	IRCF1	IRCF0

Note: more bits' default state, please refer to Table 2.3.

IRCF2:IRCF0: Internal RC oscillator frequency select bits.

IRCF2:IRCF0			Description
0	0	0	8MHZ
0	0	1	4MHZ
0	1	0	2MHZ
0	1	1	1MHZ
1	0	0	500KHZ
1	0	1	250KHZ
Other			No function, do not use.

CPUS: CPU clock source select bit.
= 0, CPU clock source is LIRC.
= 1, CPU clock source is HIRC, frequency defined by IRCF<2:0> bits.

WDTSEL1:WDTSEL0: Watchdog time-out select bits.

WDTSEL1:WDTSEL0		Time-out
0	0	2Sec
0	1	288mS
1	0	72mS
1	1	18mS

IRCEN: Internal RC enable bit
= 0, Disable internal RC clock source (Power down HIRC).
= 1, Enable internal RC clock source.
Note: Make sure the system clock (F_{CPU}) been switch to LIRC source before power down internal RC.

WDTEN: Watchdog Timer enable bit.
= 0, WDT Disable.
= 1, WDT Enable.

2.1.10 LVDTCON (LVDT Control Register)

Read/Write-POR		R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x0D	LVDTCON	EIS	RDPORT	IOB3EN	LVREN	INTEDG	LVDSEL2	LVDSEL1	LVDSEL0

Note: more bits' default state, please refer to Table 2.3.

LVDSEL2:LVDSEL0: Low voltage detects select bits.

LVDSEL2:LVDSEL0			Description
0	0	0	2.6V
0	0	1	2.4V
0	1	0	2.2V
0	1	1	1.8V
1	0	0	3.6V
1	0	1	2.0V
1	1	0	2.0V, Disable by Sleep
1	1	1	Disable

INTEDG: Interrupt edge select bit.
= 0, interrupt on falling edge of INT pin.
= 1, interrupt on rising edge of INT pin.

LVREN: LVDT reset function select bit.
= 0, Enable LVDT reset chip, reset voltage define by LVDSEL<2:0>.
= 1, Disable LVDT reset chip.

IOB3EN: IOB3/RSTB function select bit.
= 0, RSTB pin is select, IOB3 state of the bit is read as "0".
= 1, IOB3 pin is select.

RDPORT: Read port control bit for output pins.
= 0, From pins.
= 1, From register.

EIS: Define the function of IOB0/INT pin.
= 0, IOB0 (bi-directional I/O pin) is selected. The path of INT is masked.
= 1, INT (external interrupt pin) is selected. In this case, the I/O control bit of IOB0 must be set to "1". The path of Port B input change of IOB0 pin is masked by hardware, the status of INT pin can also be read by way of reading PORTB.

2.1.11 INTEN (Interrupt Mask Register)

Read/Write-POR		R/W-0	-	-	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x0E	INTEN	GIE	-	-	LVDTIE	CMPIE	INTIE	RFCIE	T1IE

Legend: - = unimplemented, read as '0'; more bits' default state, please refer to Table 2.3.

T1IE: Timer1 overflow interrupt enable bit.
= 0, Disable the Timer1 overflow interrupt.
= 1, Enable the Timer1 overflow interrupt.

INTIE: External INT pin interrupt enable bit.
= 0, Disable the External INT pin interrupt.
= 1, Enable the External INT pin interrupt.

RFCIE: RFC module interrupt enable bit.
= 0, Disable the RFC module interrupt.
= 1, Enable the RFC module interrupt.

CMPIE: Comparator change interrupt enable bit.
= 0, Disable the comparator output change interrupt.
= 1, Enable the comparator output change interrupt.

LVDTIE: LVDT interrupt enable bit.
= 0, Disable the LVDT falling edge interrupt.
= 1, Enable the LVDT falling edge interrupt.

GIE: Global interrupt enable bit.
= 0, Disable all interrupts. For wake-up from SLEEP mode through an interrupt event, the device will continue execution at the instruction after the SLEEP instruction.
= 1, Enable all un-masked interrupts. For wake-up from SLEEP mode through an interrupt event, the device will branch to the interrupt address (0x008).
Note: When an interrupt event occurs with the GIE bit and its corresponding interrupt enable bit are all set, the GIE bit will be cleared by hardware to disable any further interrupts. The RETFIE instruction will exit the interrupt routine and set the GIE bit to re-enable interrupt.

2.1.12 INTFLAG (Interrupt Status Register)

Read/Write-POR		-	-	-	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x0F	INTFLAG	-	-	-	LVDTIF	CMPIF	INTIF	RFCIF	T1IF

Legend: - = unimplemented, read as '0'; more bits' default state, please refer to Table 2.3.

T1IF: Timer1 overflow interrupt flag. Set when TMR1 overflows, reset by software.

RFCIF: RFC module interrupt flag. Set when RFC conversion is completed if RFCMOD = 0, reset by software.

INTIF: External INT pin interrupt flag. Set by rising/falling (selected by INTEDG bit (LVDTCON<6>)) edge on INT pin, reset by software.

LVDTIF: LVDT interrupt flag. Set when V_{DD} under LVDT level, reset by software.

2.1.13 PWMCON (PWM Control Register) (BANK0 & 1)

Read/Write-POR		-	-	-	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x10	PWMCON	-	-	-	PWMCS2	PWMCS1	PWMCS0	P1EN	P0EN

Legend: - = unimplemented, read as '0'; more bits' default state, please refer to Table 2.3.

P0EN: PWM0 module enable bit.
= 0, Disable PWM0 output, IOA1/PWM0 pin is configured to IOA1 pin.
= 1, Enable PWM0 output, IOA1/PWM0 pin is configured to PWM0 pin.

P1EN: PWM1 module enable bit.
= 0, Disable PWM1 output, IOA2/PWM1 pin is configured to IOA2 pin.
= 1, Enable PWM1 output, IOA2/PWM1 pin is configured to PWM1 pin.

PWMCS2:PWMCS0: PWM clock source select bits.

PWMCS2:PWMCS0			PWM1 & 2 clock source
0	0	0	8MHZ
0	0	1	4MHZ
0	1	0	2MHZ
0	1	1	1MHZ
1	0	0	500KHZ
1	0	1	250KHZ
1	1	0	125KHZ
1	1	1	No function

2.1.14 P0DPR (PWM0 Duty compare Pre-set Register) (BANK0 & 1)

Read/Write-POR		R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x011	P0DPR	PWM0 Duty Compare Pre-set register							

Legend: x = unknown, more bits' default state, please refer to Table 2.3.

P0DPR is PWM0 duty-cycle compare value pre-set register; see section 2.4 for detail description.

2.1.15 P1DPR (PWM1 Duty compare Pre-set Register) (BANK0 & 1)

Read/Write-POR		R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x012	P1DPR	PWM1 Duty Compare Pre-set register							

Legend: x = unknown, more bits' default state, please refer to Table 2.3.

P1DPR is PWM1 duty-cycle compare value pre-set register; see section 2.4 for detail description.

2.1.16 RFCCON (RFC Control Register) (BANK0 & 1)

Read/Write-POR		R/W-0	R/W-0	-	R/W-0	-	-	R/W-0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x013	RFCCON	RFCON	START	-	RFCMOD	-	-	RFCS1	RFCS0

Legend: - = unimplemented, read as '0'; more bits' default state, please refer to Table 2.3.

RFCS1:RFCS0: Select one the RFC oscillation network of RFCx (x = 0 to 2). The selected RFCx pin will be configured as output pin if RFCON = 1. Other RFCx pins will behave as tristate input pins. If RFCON = 0, all RFCx pins will behave as tristate input pins.

RFCS1:RFCS0		RFC channel
0	0	RFC0 pin is selected.
0	1	RFC1 pin is selected.
1	0	RFC2 pin is selected.
1	1	No function, don't use.

RFCMOD: RFC mode selection bit.
= 0, Enable/disable the counter by CX signal, and the clock source of the counter is the internal system clock (F_{CPU}).
= 1, Enable/disable the counter by START bit, and the clock source of the counter is the CX signal.

START: RFC counter enable bit.
= 0, Stop the RFC conversion, reset by hardware when conversion is finished or by software.
= 1, RFC counter start to convert.

RFCON: RFC module enable bit
= 0, Disable RFC module, all the RFCx and CX pins will behave as tristate input pins.
= 1, Enable RFC module.

2.1.17 RFCDLB and RFCDHB (RFC Data Register Low Byte and High Byte) (BANK0 & 1)

Read/Write-POR		R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x14	RFCDLB	Low byte of 15 bit RFC conversion result							

Read/Write-POR		R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x15	RFCDHB	RFCOV	RFCD14	RFCD13	RFCD12	RFCD11	RFCD10	RFCD9	RFCD8

Note: more bits' default state, please refer to Table 2.3.

RFCD14:RFCD0: RFC conversion result.

RFCOV: RFC counter overflow flag. Set when RFC counter overflow, reset by RFC counter reset.
= 0, Not overflow.
= 1, Overflow.

2.1.18 AWUCON (PORTA Wakeup Control Register) (BANK2 & 3)

Read/Write-POR		-	-	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x010	AWUCON	-	-	WUA5	WUA4	WUA3	WUA2	WUA1	WUA0

Legend: - = unimplemented, read as '0'; more bits' default state, please refer to Table 2.3.

WUA0: = 0, Disable the input change interrupt/wake-up function of IOA0 pin.
= 1, Enable the input change interrupt/wake-up function of IOA0 pin.

WUA1: = 0, Disable the input change interrupt/wake-up function of IOA1 pin.
= 1, Enable the input change interrupt/wake-up function of IOA1 pin.

WUA2: = 0, Disable the input change interrupt/wake-up function of IOA2 pin.
= 1, Enable the input change interrupt/wake-up function of IOA2 pin.

WUA3: = 0, Disable the input change interrupt/wake-up function of IOA3 pin.
= 1, Enable the input change interrupt/wake-up function of IOA3 pin.

WUA4: = 0, Disable the input change interrupt/wake-up function of IOA4 pin.
= 1, Enable the input change interrupt/wake-up function of IOA4 pin.

WUA5: = 0, Disable the input change interrupt/wake-up function of IOA5 pin.
= 1, Enable the input change interrupt/wake-up function of IOA5 pin.

2.1.19 APHCON (PORTA Pull-high Control Register) (BANK2 & 3)

Read/Write-POR		-	-	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x011	APHCON	-	-	/PHA5	/PHA4	/PHA3	/PHA2	/PHA1	/PHA0

Legend: - = unimplemented, read as '0'; more bits' default state, please refer to Table 2.3.

/PHA0: = 0, Enable the internal pull-high of IOA0 pin.
= 1, Disable the internal pull-high of IOA0 pin.

/PHA1: = 0, Enable the internal pull-high of IOA1 pin.
= 1, Disable the internal pull-high of IOA1 pin.

/PHA2: = 0, Enable the internal pull-high of IOA2 pin.
= 1, Disable the internal pull-high of IOA2 pin.

/PHA3: = 0, Enable the internal pull-high of IOA3 pin.
= 1, Disable the internal pull-high of IOA3 pin.

/PHA4: = 0, Enable the internal pull-high of IOA4 pin.
= 1, Disable the internal pull-high of IOA4 pin.

/PHA5: = 0, Enable the internal pull-high of IOA5 pin.
= 1, Disable the internal pull-high of IOA5 pin.

2.1.20 BWUCON (PORTB Wakeup Control Register) (BANK2 & 3)

Read/Write-POR		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x012	BWUCON	WUB7	WUB6	WUB5	WUB4	WUB3	WUB2	WUB1	WUB0

Legend: - = unimplemented, read as '0'; more bits' default state, please refer to Table 2.3.

WUB0: = 0, Disable the input change interrupt/wake-up function of IOB0 pin.
= 1, Enable the input change interrupt/wake-up function of IOB0 pin.

WUB1: = 0, Disable the input change interrupt/wake-up function of IOB1 pin.
= 1, Enable the input change interrupt/wake-up function of IOB1 pin.

WUB2: = 0, Disable the input change interrupt/wake-up function of IOB2 pin.
= 1, Enable the input change interrupt/wake-up function of IOB2 pin.

WUB3: = 0, Disable the input change interrupt/wake-up function of IOB3 pin.
= 1, Enable the input change interrupt/wake-up function of IOB3 pin.

WUB4: = 0, Disable the input change interrupt/wake-up function of IOB4 pin.
= 1, Enable the input change interrupt/wake-up function of IOB4 pin.

WUB5: = 0, Disable the input change interrupt/wake-up function of IOB5 pin.
= 1, Enable the input change interrupt/wake-up function of IOB5 pin.

WUB6: = 0, Disable the input change interrupt/wake-up function of IOB6 pin.
= 1, Enable the input change interrupt/wake-up function of IOB6 pin.

WUB7: = 0, Disable the input change interrupt/wake-up function of IOB7 pin.
= 1, Enable the input change interrupt/wake-up function of IOB7 pin.

2.1.21 BPHCON (PORTB Pull-high Control Register) (BANK2 & 3)

Read/Write-POR		R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x013	BPHCON	/PHB7	/PHB6	/PHB5	/PHB4	GP	/PHB2	/PHB1	/PHB0

Note: more bits' default state, please refer to Table 2.3.

/PHB0: = 0, Enable the internal pull-high of IOB0 pin.
= 1, Disable the internal pull-high of IOB0 pin.

/PHB1: = 0, Enable the internal pull-high of IOB1 pin.
= 1, Disable the internal pull-high of IOB1 pin.

/PHB2: = 0, Enable the internal pull-high of IOB2 pin.
= 1, Disable the internal pull-high of IOB2 pin.

GP: General purpose read/write bits.

/PHB4: = 0, Enable the internal pull-high of IOB4 pin.
= 1, Disable the internal pull-high of IOB4 pin.

/PHB5: = 0, Enable the internal pull-high of IOB5 pin.
= 1, Disable the internal pull-high of IOB5 pin.

/PHB6: = 0, Enable the internal pull-high of IOB6 pin.
= 1, Disable the internal pull-high of IOB6 pin.

/PHB7: = 0, Enable the internal pull-high of IOB7 pin.
= 1, Disable the internal pull-high of IOB7 pin.

2.1.22 CMPCON1 (Comparator Control Register1)

Read/Write-POR		-	-	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x014	CMPCON1	-	-	COUT	CINV	CINS	CM2	CM1	CM0

Legend: - = unimplemented, read as '0'; more bits' default state, please refer to Table 2.3.

CM2:CM0: Comparator mode select bits. See Figure 2.10 for detail description.

CM2:CM0			Comparator mode
0	0	0	Comparator Off (lowest power).
0	0	1	
0	1	0	
0	1	1	Comparator Reset (low power).
1	0	0	Multiplexed Input with CV_{REF}.
1	0	1	Multiplexed Input with Bandgap.
1	1	0	Comparator with CV_{REF} & Bandgap.
1	1	1	Comparator with IOB7 & IOB6.

CINS: Comparator input switch bit.
When CM2:CM0 = 100 or 101:
= 0, VIN- connects to CIN-.
= 1, VIN- connects to CIN+.
Other modes:
Ignore.

CINV: Comparator output polarity inversion bit.
= 0, Output not inverted.
= 1, Output inverted.

COUT: Comparator output bit.
If C1INV = 0: = 0, VIN+ < VIN-.
= 1, VIN+ > VIN-.
If C1INV = 1: = 0, VIN+ > VIN-.
= 1, VIN+ < VIN-.

2.1.23 CMPCON2 (Comparator Control Register2)

Read/Write-POR		-	-	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x15	CMPCON2	-	-	CVREN	CVRR	CVR3	CVR2	CVR1	CVR0

Legend: - = unimplemented, read as '0'; more bits' default state, please refer to Table 2.3.

CVR3:CVR0: Comparator voltage reference (CV_{REF}) select bits.

If CVRR = 1 (low range): $CV_{REF} = \frac{(CVR3:CVR0)*V_{DD}}{18}$

If CVRR = 0 (high range): $CV_{REF} = \frac{V_{DD}}{10} + \frac{(CVR3:CVR0)*V_{DD}}{20}$

CVRR: CV_{REF} range selection bit.
= 0, High range.
= 1, Low range.

CVREN: Comparator voltage reference (CV_{REF}) module enable bit.
= 0, Disable CV_{REF} module.
= 1, Enable CV_{REF} module.

2.1.24 PCHBUF (High Byte Buffer of Program Counter)

Read/Write-POR		-	-	-	-	-	-	W-0	W-0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x16	PCHBUF	-	-	-	-	-	-	2 MSBs Buffer of PC	

Legend: - = unimplemented, read as '0', more bits' default state, please refer to Table 2.3.

Bit1:Bit0: See 2.1.2 for detail description.

2.1.25 ACC (Accumulator)

Read/Write-POR		R/W-x							
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
N/A	ACC	Accumulator							

Legend: x = unknown, more bits' default state, please refer to Table 2.3.

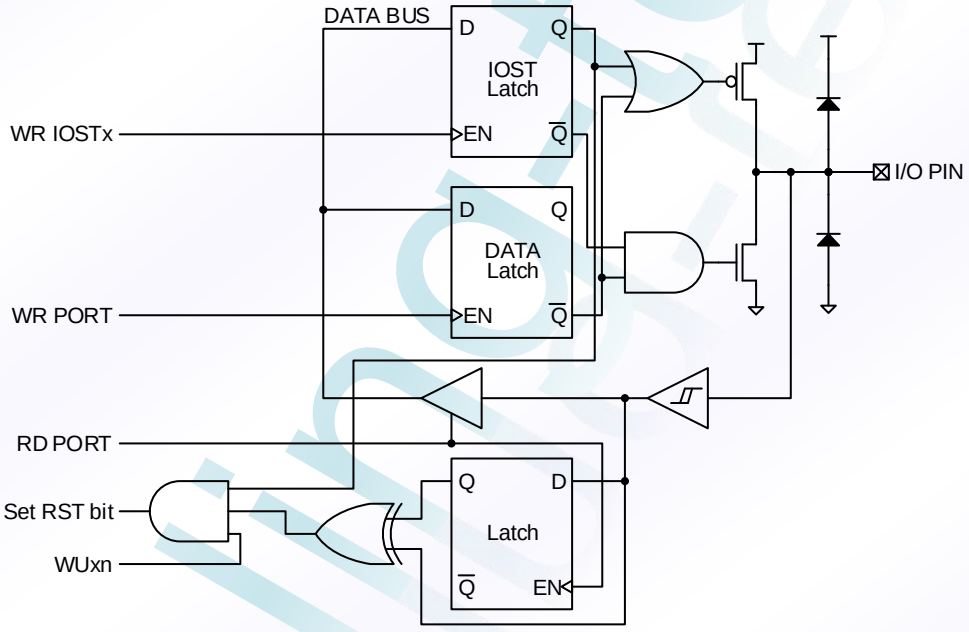
Accumulator is an internal data transfer, or instruction operand holding. It cannot be addressed.

2.2 I/O Ports

PORTA and PORTB are bi-directional tristate I/O ports. PORTA are 6-pin I/O port, PORTB are 8-pin I/O port. Please note that IOB3 is an input or open-drain output pin.
All I/O pins have data direction control registers (IOSTA, IOSTB) which can configure these pins as output or input. IOA<5:0>, IOB<5:4> and IOB<2:0> have its corresponding pull-high control bits (APHCON and BPHCON register) to enable the weak internal pull-high. The weak pull-high is automatically turned off when the pin is configured as an output pin.
All I/O pins also provides the input change interrupt/wake-up function. Each pin has its corresponding input change interrupt/wake-up enable bits (AWUCON and BWUCON) to select the input change interrupt/wake-up source.
The IOB0 is also an external interrupt input signal.
Please note, IOB3 voltage on these pins must not exceed V_{DD}, otherwise it will cause the pin breakdown.

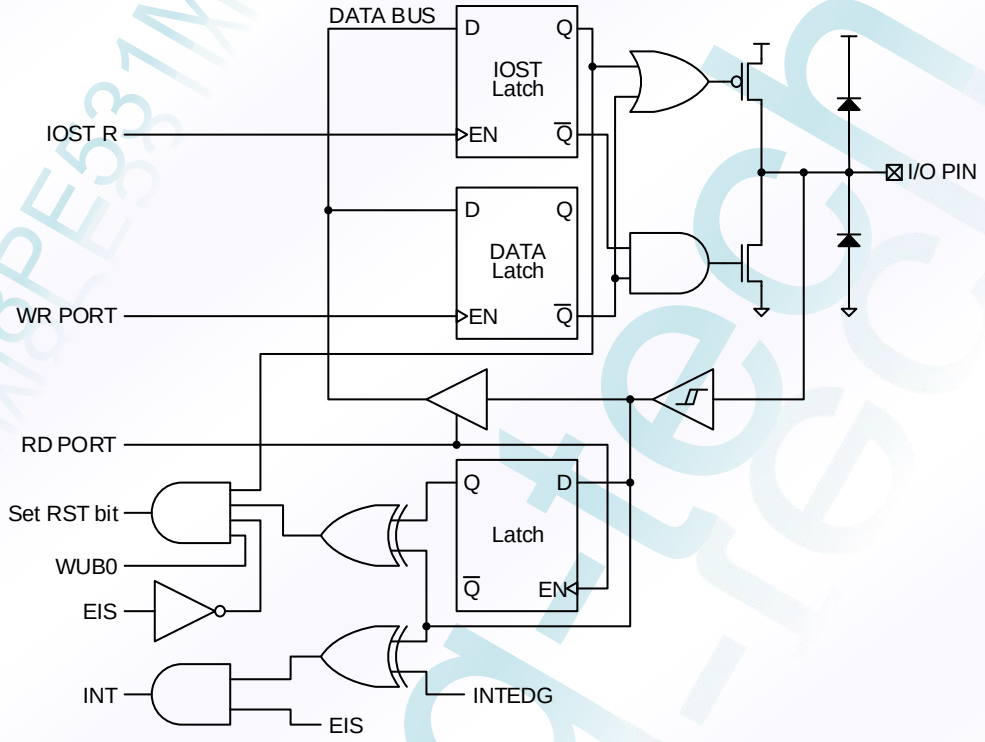
Figure 2.3: Block Diagram of I/O Pins

IOA5 ~ IOA0, IOB5, IOB4, IOB2, IOB1:



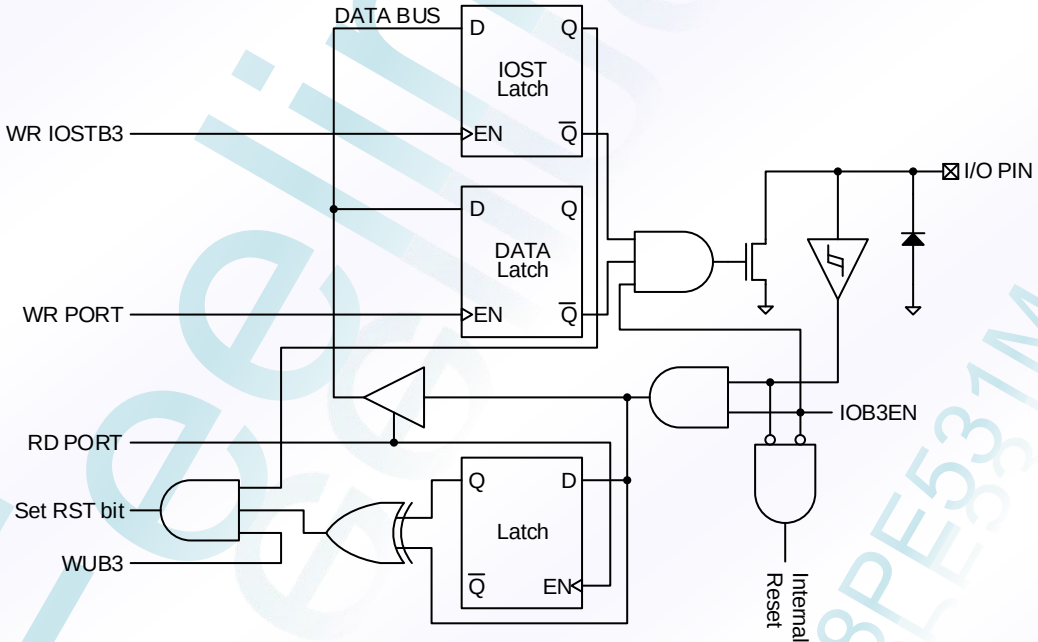
Pull-high are not shown in this figure

IOB0:



Pull-high are not shown in this figure

IOB3:



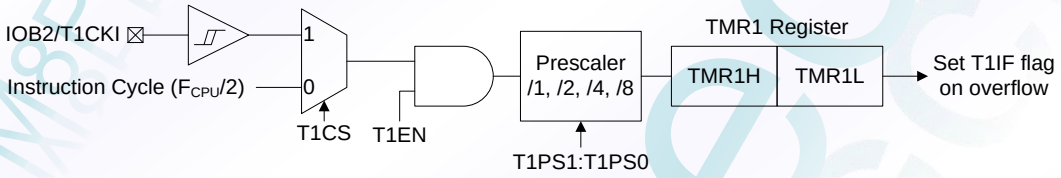
Voltage on this pin must not exceed V_{DD}.

2.3 Timer1

The Timer1 is a 16-bit timer/counter with the following features:

- Readable and writable.
- Internal or external clock selection.
- Asynchronous operation.
- Interrupt on overflow from 0xFFFF to 0x0000.
- Wake-up upon overflow

Figure 2.4: Block Diagram of the Timer1



2.3.1 Timer1 Pre-scaler

Timer1 has four pre-scaler options allowing 1, 2, 4, or 8 divisions of the clock input. The T1PS<1:0> bits (T1CON<4:3>) control the pre-scaler counter. The pre-scaler counter is not directly readable or writable; however, the pre-scaler counter is cleared upon a write to TMR1HB or TMR1LB.

2.3.1.1 Using Timer1 with an Internal Clock: Timer mode

Timer mode is selected by clearing the T1CS bit (T1CON<1>). In timer mode, the timer1 register (TMR1HB and TMR1LB) will increment every instruction cycle (pre-scaler ratio is 1:1).

2.3.1.2 Using Timer1 with an External Clock: Counter mode

Counter mode is selected by setting the T1CS bit (T1CON<1>). In this mode, Timer1 will increment either on every rising edge of pin T1CKI.
In this mode, the external clock input is not synchronized. The timer continues to increment asynchronous to the internal phase clocks. The timer will continue to run during SLEEP and can generate an interrupt on overflow, which will wake-up the processor. However, special precautions in software are needed to read/write the timer.
Reading TMR1HB or TMR1LB, while the timer is running from an external asynchronous clock, will ensure a valid read (taken care of in hardware). However, the user should keep in mind that reading the 16-bit timer in two 8-bit values itself, poses certain problems, since the timer may overflow between the reads.
For writes, it is recommended that the user simply stop the timer and write the desired values. A write contention may occur by writing to the timer registers, while the register is incrementing. This may produce an unpredictable value in the timer register.

2.3.2 Timer1 Operation During SLEEP

Timer1 can be operate during SLEEP mode. In this mode, an external clock source can be used to increment the counter.
The device will wake-up on an overflow. If the GIE bit (INTEN<7>) is set, the device will wake-up and jump to the interrupt vector. If the GIE bit is cleared, the device will wake-up and continue execution at the instruction after the SLEEP instruction.

2.4 Pulse Width Modulation (PWM)

FM8PE531M provides two PWM output shared with IOA1/PWM0 and IOA2/PWM1 pins. These PWM period-time are fixed and cannot be programmable.
The PWM0 and PWM1 outputs has a maximum resolution of 8-bits, the duty cycle of the output can vary from 0% to 99%.

The PWM0 and PWM1 period time can be calculated as follows:

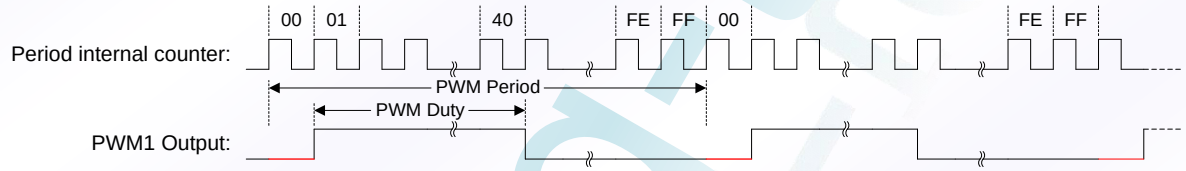
$$\text{Period time of PWM} = \frac{256}{\text{PWM Clock source frequency}}$$

The PWM0 duty cycle time can be calculated as follows:

$$\text{Duty cycle time of PWM0} = \frac{\text{P0DPR}}{\text{PWM Clock source frequency}}$$

Similarly, this formula can be used directly on PWM1.

Figure 2.5: PWM0 Output Waveform



Note: Red line will be fixed output “LOW”.

Example 2.2: PWM0 & PWM1Setting

ASM Language Code

```
#include   <8PE531M.ASH>
           …
           MOVIA    0x40
           MOVAR    P0DPR          ; PWM0 Duty time = 0x40 / 8MHZ = 8uS

           MOVIA    0x80
           MOVAR    P1DPR          ; PWM1 Duty time = 0x80 / 8MHZ = 16uS

           MOVIA    0x03           ; PWM Clock source to 8MHZ, and Enable PWM0 & PWM1 output
           MOVAR    PWMCON         ; Period cycle = 256 / 8MHZ = 32uS
           …
```

C Language Code

```
#include   <8PE531M.h>
           …
           P0DPR=0x40;              // PWM0 Duty time = 0x40 / 8MHZ = 8uS

           P1DPR=0x80;              // PWM1 Duty time = 0x80 / 8MHZ =16uS

           PWMCON=0x03;             // PWM Clock source to 8MHZ, and enable PWM0 & PWM1 output
                                    // Period cycle = 256 / 8MHZ = 32uS
           …
```

2.5 Resistor to Frequency Converter (RFC)

The Resistor to Frequency Converter (RFC) can compare two different sensors with the reference resistor separately.
This RFC contains four external pins:
CX: the oscillation Schmitt trigger input (IOA3/CX pin).
RFC0 ~ RFC2: the resistor/sensor output pin 0 ~ 2 (RFC0, RFC1, and RFC2 pins)

Figure 2.6: The Block Diagram of RFC

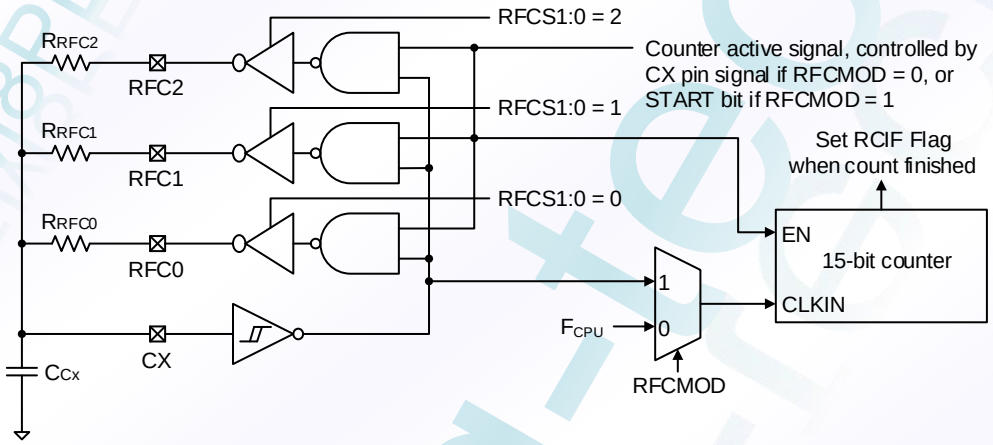


Table 2.1: The Description of RFC Control Bits

RFCS1:RFCS0	Select one the RFC oscillation network of RFCx (x = 0 to 2). The selected RFCx pin will be configured as RFCx output pin if RFCON = 1. Other RFCx pins will still behave as tristate input pins. If RFCON = 0, all RFCx pins will behave as tristate input pins.
RFCMOD	= 0, Enable/disable the counter by CX signal, and the clock source of the counter is the internal system clock (F_{CPU}). = 1, Enable/disable the counter by START bit, and the clock source of the counter is the CX signal.
START	= 0, Stop the RFC conversion = 1, RFC counter start to convert. Reset by hardware after conversion is finished. Note: Don't clear START bit by software during the RFC conversion.
RFCON	= 0, Disable RFC module, all the RFCx and CX pins will behave as tristate input pins. = 1, Enable RFC module.

2.5.1 RC Oscillator Network

The RFC circuitry may build up 3 RC oscillation networks through RFC0 to RFC2 and CX pins with external resistors. Only one RC oscillation network may be active at a time. When the oscillation network is built up, the count active pulse will be generated by the oscillation network and transferred to the 15-bit counter through the CX pin. It will then enable or disable the 15-bit counter in order to count the oscillation clock. **The 15-bit RFC counter is cleared when a value is written to RFCCON register, RFCON bit is cleared, and during any kind of reset as well.**

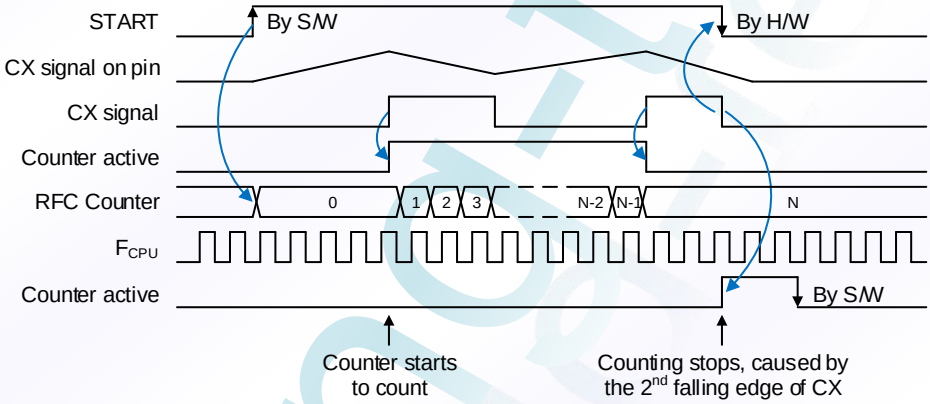
How to build the RC oscillation network?
1. Connect the resistor and capacitor on RFCx (x = 0 to 2, if needed) and CX pins.
2. Switch all of the needed RFCx and CX pins to input mode.
3. Enable the RFC module by set the RFCON bit.
4. Select one of RFCx pins by RFCS1:RFCS0 bits to enable the output pin for RC networks respectively. The selected RFCx will output low at this time. Other RFCx pins will become of a tristate type.

5. Set START bit to enable the RC oscillation network and 15-bit counter. The RC oscillation network will not operate if this bit has not been set. If RFCMOD bit = 0, Clear the START bit by H/W will finish the conversion, and the RFCIF flag will be set (if enable interrupt). If RFCMOD bit = 1, Clear the START bit by S/W will finish the conversion, and the RFCIF flag will not be set.

2.5.2 Enable/Disable the Counter by CX Signal

In this mode, CX pin is the signal to control the counter period and the clock source of the counter comes from the internal system clock (F_{CPU}).
The counter will start to count after the first rising edge signal applied on the CX pin after the RFCON bit (RFCCON<7>) is set. Once the second rising edge is applied to the CX pin after the counter is enabled, the counter will stop counting. And after the second falling edge is applied to the CX pin, the RFC block will clear the START bit and set the RFC interrupt flag RFCIF bit (INTFLAG<1>) if RFCIE bit (INTEN<1>) is set.
User also can be polling the RFCON or RFCIF bit to check if the conversion is finished.

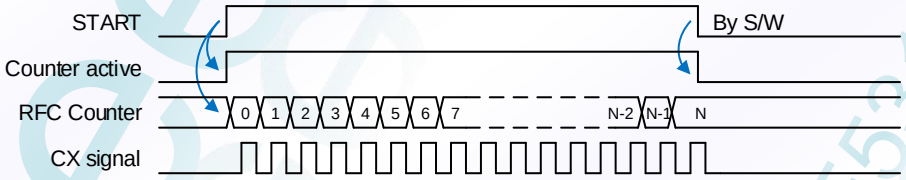
Figure 2.7: The Sample of the RFC Counter Controlled by the CX Pin (RFCMOD = 0)



2.5.3 Enable/Disable the Counter by START Bit

In this mode, START bit is the signal to control the counter period and the clock source of the counter comes from the CX pin.
The counter will start to count after the START bit (RFCCON<6>) is set. Once the START bit is cleared by S/W, the counter will stop counting. In this case, the RFC interrupt flag RFCIF bit (INTFLAG<1>) will not be set.

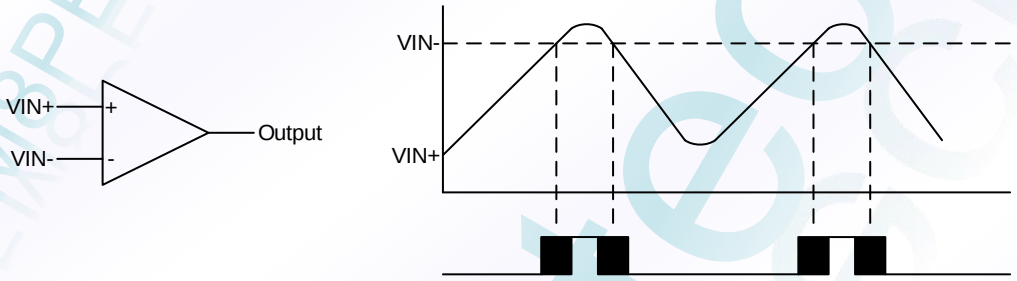
Figure 2.8: The Sample of the RFC Counter Controlled by the START Bit (RFCMOD = 1)



2.6 Comparator Module

The FM8PE513M device has one comparator. The inputs to the comparator is multiplexed with the IOB6 and IOB7 pins. There is an on-chip comparator voltage reference (CV_{REF} and Bandgap) that can also be applied to an input of these comparators.
The compared results are stored in the COUT bit of CMPCON1 register. This bit is read-only.
All pins configured as comparator analog inputs will read as a '0's.

Figure 2.9: Single Comparator



2.6.1 Comparator Output State

Comparator output state can be read internally via the COUT bit of the CMPCON1 register.

2.6.2 Comparator Output Polarity

The polarity of the comparator output can be inverted by setting the CINV bit of the CMPCON1 register. Clearing CINV bit to "0" results in a non-inverted output. Setting CINV bit to "1" results in a polarity inverted output.

Table 2.2: COUT Status/Output vs. Input Conditions & CINV

Input Conditions	Comparator Output	CINV	COUT
VIN+ < VIN-	0	0	0
VIN+ > VIN-	1	0	1
VIN+ < VIN-	0	1	1
VIN+ > VIN-	1	1	0

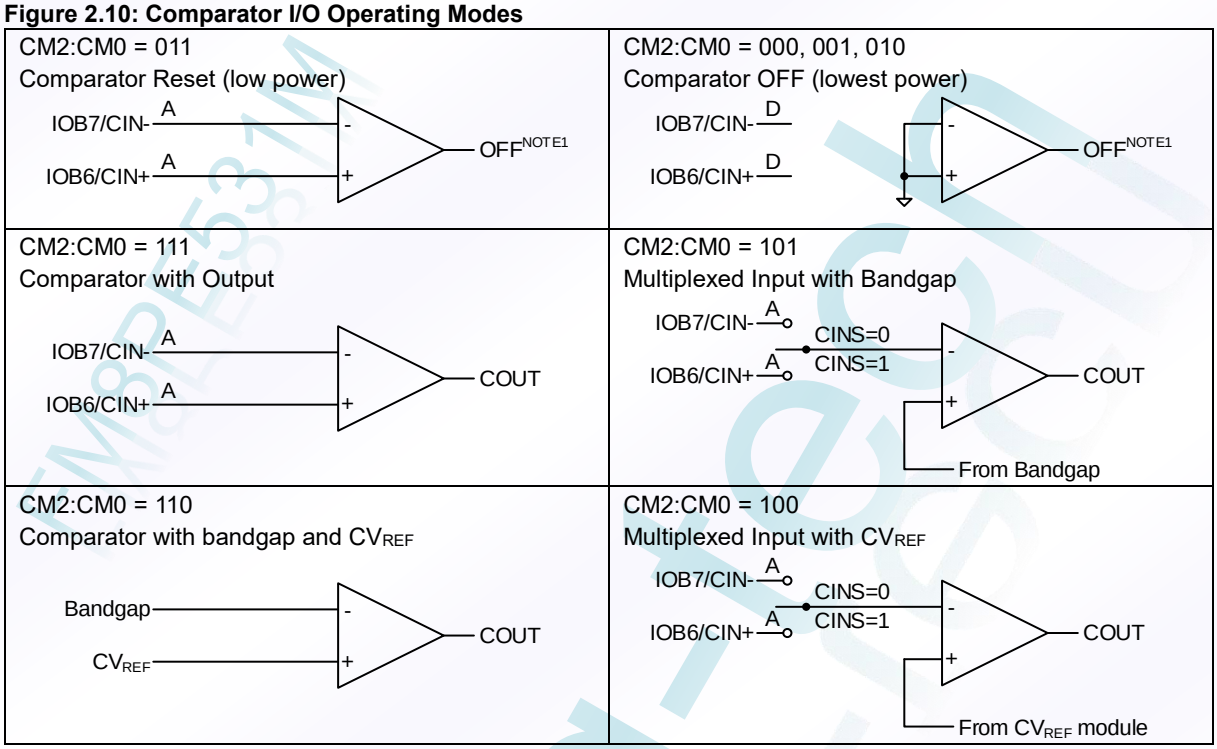
2.6.3 Comparator Input Switch

The inverting input (VIN-) of the comparators may be switched between two analog pins if CM<2:0> = 100 or 101. In these modes, both pins remain in analog mode regardless of which pin is selected as the input. The CINS bit of the CMPCON1 register controls the comparator input switch.

2.6.4 Comparator Operating Modes

There are six modes of operation for the comparator. The CM<2:0> bits of CMPCON1 register used to select these modes.
The pins denoted as "A" will read as a "0" regardless the state of the I/O pin or the I/O control IOSTBx bit. If pins are used as comparator analog inputs, the corresponding IOSTBx bit must be set to "1".
Pins denoted as "D" means pins not used as comparator, these pins are normal I/O pin.
If the comparator mode is changed, the comparator output level may not be valid for a specified period of time, so comparator interrupts should be disabled during a comparator mode change.

Figure 2.10: Comparator I/O Operating Modes



Note1: Reads as "0".

Note2: A = Comparator analog input, pins always read '0'. D = Digital I/O.

CINS = Comparator input switch select bit (CMPCON1<3>).

COUT = Comparator output bit (CMPCON1<5>).

2.6.5 Comparator Voltage Reference (CV_{REF})

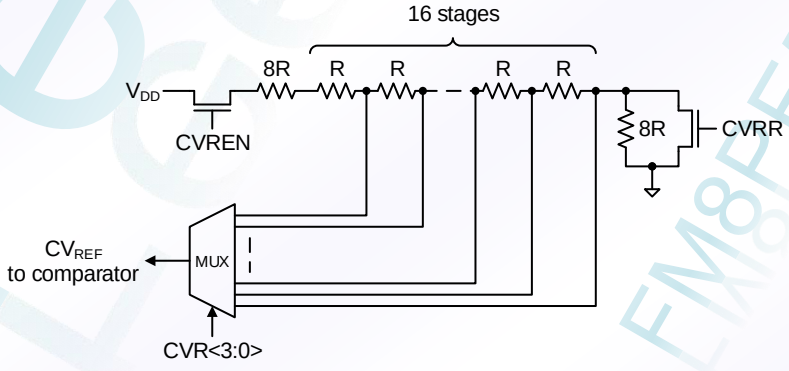
The comparator module also allows the selection of an internally generated voltage reference for one of the comparator inputs. The internal reference signal is used for three of the six comparator modes. The CMPCON2 register controls the voltage reference module.

The voltage reference can output 32 distinct voltage levels, 16 in a high range and 16 in a low range. The following equations determine the output voltages:

$$\text{If CVRR = 1 (low range): } CV_{REF} = \frac{(CVR3:CVR0)*V_{DD}}{18}$$

$$\text{If CVRR = 0 (high range): } CV_{REF} = \frac{V_{DD}}{10} + \frac{(CVR3:CVR0)*V_{DD}}{20}$$

Figure 2.11: Comparator Voltage Reference



2.7 Interrupts

The FM8PE531M has up to four sources of interrupt:
1. Timer1 overflow interrupt.
2. RFC module interrupt.
3. External interrupt INT pin.
4. Comparator interrupt.
5. Programmable voltage LVDT interrupt.
6. PORTA and PORTB external interrupt.

INTFLAG is the interrupt flag register that recodes the interrupt requests in the relative flags.
A global interrupt enable bit, GIE (INTEN<7>), enables (if set) all un-masked interrupts or disables (if cleared) all interrupts. Individual interrupts can be enabled/disabled through their corresponding enable bits in INTEN register regardless of the status of the GIE bit.
When an interrupt event occurs with the GIE bit and its corresponding interrupt enable bit are all set, the GIE bit will be cleared by hardware to disable any further interrupts, and the next instruction will be fetched from address 0x008.
The interrupt flag bits must be cleared by software before re-enabling GIE bit to avoid recursive interrupts.
The RETFIE instruction exits the interrupt routine and set the GIE bit to re-enable interrupt.

2.7.1 Timer1 Interrupt

An overflow (0xFFFF → 0x0000) in the TMR1HB:TMR1LB register pair will set the flag bit T1IF (INTFLAG<0>). To enable the interrupt, T1IE bit (INTEN<0>), and GIE bit (INTEN<7>) should be set.
The T1IF bit must be cleared by software before re-enabling this interrupt.

2.7.2 RFC Module Interrupt

After RFC conversion is finished, the RFCIF flag (INTFLAG<1>) will be set. This interrupt can be disabled by clearing RFCIE bit (INTEN<1>).
The RFC interrupt only for CX mode (RFCMOD=0).

2.7.3 External INT Interrupt

External interrupt on INT pin is rising or falling edge triggered selected by INTEDG (LVDTCON<3>).
When a valid edge appears on the INT pin the flag bit INTIF (INTFLAG<2>) is set.
The INTIE bit (INTEN<2>) and GIE bit (INTEN<7>) must be set to enable the interrupt. If any of these bits cleared, the interrupt is not enable.
The INT pin interrupt can wake-up the system from SLEEP condition, if bit INTIE was set before going to SLEEP. If GIE bit was set, the program will execute interrupt service routine after wake-up; or if GIE bit cleared, the program will execute next PC after wake-up.

2.7.4 Comparator Status Change Interrupt

The comparator interrupt flag bit CMPIF (INTFLAG<3>) is set whenever there is a change in the output value of the comparator.
The CMPIE bit (INTEN<3>) and GIE bit (INTEN<7>) must be set to enable the interrupt. If any of these bits cleared, the interrupt is not enable.

2.7.5 Programmable voltage LVDT interrupt

When the V_{DD} voltage drops below programmed voltage (Selection by LVDTSEL<2:0> bits (LVDTCON<2:0>)), flag bit LVDTIF (INTFLAG<4>) will be set. In addition, the LVDTIF bit can be clear by software.
The LVDTIE bit (INTEN<4>), LVREN bit (LVDTCON<4>), and GIE bit (INTEN<7>) must be set to enable the interrupt. If any of these bits cleared, the interrupt is not enable.

2.7.6 PORTA and PORTB external Interrupt

Before the PORTA and PORTB input change interrupt are enable, reading PORTA and PORTB (any instruction accessed to PORTA and PORTB, including read/write instructions) is necessary. Any pin which corresponding WUAn (AWUCON<5:0>) or WUBn bit (BWUCON<7:0>) is cleared to “0” or configured as output or IOB0 pin configured as INT pin will be excluded from this function.
The PORTA and PORTB input change interrupt also can wake-up the system from SLEEP condition, the GIE bit decides whether the processor branches to the interrupt vector following wake-up. If GIE bit was set, the program will execute interrupt service routine after wake-up; or if GIE bit cleared, the program will execute next PC after wake-up.

2.8 Power-down Mode (SLEEP)

Power-down mode is entered by executing a SLEEP instruction.
When SLEEP instruction is executed, the $\overline{PD}$ bit (STATUS<3>) is cleared, the $\overline{TO}$ bit is set, the watchdog timer will be cleared and keeps running, and the oscillator driver is turned off.
All I/O pins maintain the status they had before the SLEEP instruction was executed.

2.8.1 Wake-up from SLEEP Mode

The device can wake-up from SLEEP mode through one of the following events:
1. RSTB reset.
2. WDT time-out wake-up (if enabled).
3. Interrupt from IOB0/INT pin, PORTA or PORTB change, or Timer1 interrupt.

External RSTB reset and WDT time-out will cause a device reset. Interrupt event is considered a continuation of program execution.
In the reset case, the $\overline{PD}$ and $\overline{TO}$ bits can be used to determine the cause of device reset. The $\overline{PD}$ bit is set on power-up and is cleared when SLEEP instruction is executed. The $\overline{TO}$ bit is cleared if a WDT time-out occurred. The RST bit is set on PORTA or PORTB input change wake-up.
For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set. Wake-up is regardless of the GIE bit. If GIE bit is cleared, the device will continue execution at the instruction after the SLEEP instruction. If the GIE bit is set, the device will branch to the interrupt address (0x008).

2.9 Reset

FM8PE531M devices may be RESET in one of the following ways:
1. Power-on Reset (POR)
2. Brown-out Reset (BOR)
3. RSTB Pin Reset
4. WDT time-out Reset during normal operation

Some registers are not affected in any RESET condition. Their status is unknown on Power-on Reset and unchanged in any other RESET. Most other registers are reset to a “reset state” on Power-on Reset, RSTB or WDT Reset.
A Power-on RESET pulse is generated on-chip when V_{DD} rise is detected. To use this feature, the user merely ties the RSTB pin to V_{DD}.
On-chip Low Voltage Detector (LVD) places the device into reset when V_{DD} is below a fixed voltage. This ensures that the device does not continue program execution outside the valid operation V_{DD} range. Brown-out RESET is typically used in AC line or heavy loads switched applications.
A RSTB or WDT time-out during normal operation also results in a device RESET.
The $\overline{PD}$ and $\overline{TO}$ bits (STATUS<4:3>) are set or cleared depending on the different reset conditions.

Table 2.3: Reset Conditions for All Registers

Register	Address	Power-on Reset Brown-out Reset	RSTB Reset WDT Reset
ACC	N/A	xxxx xxxx	xxxx xxxx
INDF	0x00	xxxx xxxx	uuuu uuuu
PCL	0x02	0000 0000	0000 0000
STATUS	0x03	0101 1xxx	010# #xxx
FSR	0x04	00xx xxxx	00uu uuuu
IOSTA	0x05	--11 1111	--11 1111
PORTA	0x06	--xx xxxx	--xx xxxx
IOSTB	0x07	1111 1111	1111 1111
PORTB	0x08	xxxx xxxx	xxxx xxxx
T1CON	0x09	---0 0000	---0 0000
TMR1LB	0x0A	0000 0000	0000 0000
TMR1HB	0x0B	0000 0000	0000 0000
OSCCON	0x0C	1111 0000	uuuu uuuu
LVDTCON	0x0D	1110 0111	uuuu uuuu
INTEN	0x0E	0--0 0000	0--0 0000
INTFLAG	0x0F	---0 0000	---0 0000
PWMCON	0x10, Bank0 & 1	---0 0000	---0 0000
P0DPR	0x11, Bank0 & 1	**xxxx xxxx**	**xxxx xxxx**
P1DPR	0x12, Bank0 & 1	**xxxx xxxx**	**xxxx xxxx**
RFCCON	0x13, Bank0 & 1	00-0 --00	00-0 --00
RFCDLB	0x14, Bank0 & 1	0000 0000	0000 0000
RFCDHB	0x15, Bank0 & 1	0000 0000	0000 0000
AWUCON	0x10, Bank2 & 3	--00 0000	--00 0000
APHCON	0x11, Bank2 & 3	--11 1111	--11 1111
BWUCON	0x12, Bank2 & 3	0000 0000	0000 0000
BPHCON	0x13, Bank2 & 3	1111 1111	1111 1111
CMPCON1	0x14, Bank2 & 3	--00 0000	--00 0000
CMPCON2	0x15, Bank2 & 3	--00 0000	--00 0000
PCHBUF	0x16	---- --00	---- --00
General Purpose Registers	0x18 ~ 0x3F	xxxx xxxx	uuuu uuuu

Legend: u = unchanged, x = unknown, - = unimplemented, read as 0.
= refer to the following table for possible values.

Table 2.4: RST / $\overline{TO}$ / $\overline{PD}$ Status after Reset or Wake-up

RST	$\overline{TO}$	$\overline{PD}$	RESET was caused by
0	1	1	Power-on Reset
0	1	1	Brown-out reset
0	u	u	RSTB Reset during normal operation
0	1	0	RSTB Reset during SLEEP
0	0	1	WDT Reset during normal operation
0	0	0	WDT Wake-up during SLEEP
1	1	0	Wake-up on pin change during SLEEP

Legend: u = unchanged

Table 2.5: Events Affecting$\overline{TO}$ / $\overline{PD}$Status Bits

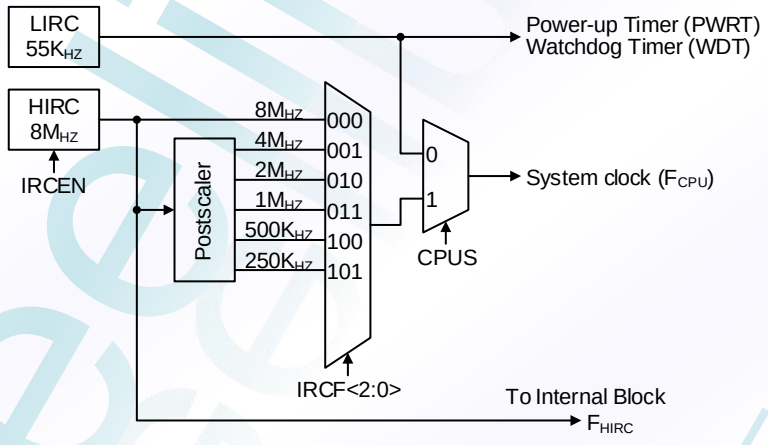
Event	$\overline{TO}$	$\overline{PD}$
Power-on	1	1
WDT Time-Out	0	u
SLEEP instruction	1	0
CLRWDT instruction	1	1

Legend: u = unchanged

2.10 Oscillator Configurations

The system clock can be generated from two internal oscillators. The HIRC ($8M_{HZ}$) is a calibrated high-frequency oscillator. The LIRC ($55K_{HZ}$) is an un-calibrated low-frequency oscillator.
The Oscillator Control register (OSCCON) controls the system clock and frequency selection options. The OSCCON register contains IRCF (frequency selection bits), CPUS (CPU clock source select bit) and IRCEN (HIRC module enable bit), see section 2.1.9 for detail description.

Figure 2.12: System Clock Source Block Diagram



2.10.1 How to change system clock speed

The system clock speed can be selected by setting the Clock Divider Select bits IRCF<2:0> of the OSCCON register.
When you want to switch clock source, Need follow these steps:

1. Switching the clock source to LIRC (CPUS bit (OSCCON<3>) set to 0).
2. Insert a NOP instruction.
3. Specify new clock speed** (see note2).
4. Insert a NOP instruction.
5. Switching the clock source to HIRC (CPUS bit (OSCCON<3>) set to 1).
6. Insert a NOP instruction.

Example 2.3: Change clock speed (Change to $4M_{HZ}$)

ASM Language Code

```
#include   <8PE531M.ASH>
           …
           BCR     OSCCON,CPUS_B      ; Switch system clock source to LIRC, required.
           NOP
           BSR     OSCCON,IRCF0_B
           BCR     OSCCON,IRCF1_B
           BCR     OSCCON,IRCF2_B     ; 4MHZ IRCF<2:0> is 001
           NOP
           BSR     OSCCON,CPUS_B      ; Switch system clock source to HIRC, required.
           NOP
           …
```

C Language Code

```
#include   <8PE531M.h>
           …
           OSCCONbits.CPUS=0;         // Switch system clock source to LIRC, required.
           NOP();
           OSCCONbits.IRCF0=1;
           OSCCONbits.IRCF1=0;
           OSCCONbits.IRCF2=0;        // 4MHZ IRCF<2:0> is 001
           NOP();
           OSCCONbits.CPUS=1;         // Switch system clock source to HIRC, required.
           NOP();
           …
```

Note: 1. OSCCON register prohibits direct write value, Need using BSR/BCR instruction.
2. When switch to another speed, setting procedures must same as example.
3. Failure to follow set procedures could result in unexpected situation occurs.

3.0 INSTRUCTION SET

Mnemonic, Operands		Description	Operation	Cycles	Status Affected
BCR	**R, bit**	Clear bit in R	0 → R<b>	1	-
BSR	**R, bit**	Set bit in R	1 → R<b>	1	-
BTRSC	**R, bit**	Test bit in R, Skip if Clear	Skip if R<b> = 0	1/2	-
BTRSS	**R, bit**	Test bit in R, Skip if Set	Skip if R<b> = 1	1/2	-
NOP		No Operation	No operation	1	-
CLRWDT		Clear Watchdog Timer	0x00 → WDT,	1	$\overline{TO}$,$\overline{PD}$
SLEEP		Go into power-down mode	0x00 → WDT, 0x00 → WDT pre-scaler	1	$\overline{TO}$,$\overline{PD}$
RETURN		Return from subroutine	Top of Stack → PC	2	-
RETFIE		Return from interrupt, set GIE bit	Top of Stack → PC, 1 → GIE	2	-
CLRA		Clear ACC	0x00 → ACC	1	Z
CLRR	**R**	Clear R	0x00 → R	1	Z
MOVAR	**R**	Move ACC to R	ACC → R	1	-
MOVR	**R, d**	Move R	R → dest	1	Z
DECR	**R, d**	Decrement R	R - 1 → dest	1	Z
DECRSZ	**R, d**	Decrement R, Skip if 0	R - 1 → dest, Skip if result = 0	1/2	-
INCR	**R, d**	Increment R	R + 1 → dest	1	Z
INCRSZ	**R, d**	Increment R, Skip if 0	R + 1 → dest, Skip if result = 0	1/2	-
ADDAR	**R, d**	Add ACC and R	R + ACC → dest	1	C, DC, Z
SUBAR	**R, d**	Subtract ACC from R	R - ACC → dest	1	C, DC, Z
ADCAR	**R, d**	Add ACC and R with Carry	R + ACC + C → dest	1	C, DC, Z
SBCAR	**R, d**	Subtract ACC from R with Carry	R + $\overline{ACC}$ + C → dest	1	C, DC, Z
ANDAR	**R, d**	AND ACC with R	ACC and R → dest	1	Z
IORAR	**R, d**	Inclusive OR ACC with R	ACC or R → dest	1	Z
XORAR	**R, d**	Exclusive OR ACC with R	R xor ACC → dest	1	Z
COMR	**R, d**	Complement R	$\bar{R}$→ dest	1	Z
RLR	**R, d**	Rotate left R through Carry	R<7> → C, R<6:0> → dest<7:1>, C → dest<0>	1	C
RRR	**R, d**	Rotate right R through Carry	C → dest<7>, R<7:1> → dest<6:0>, R<0> → C	1	C
SWAPR	**R, d**	Swap R	R<3:0> → dest<7:4>, R<7:4> → dest<3:0>	1	-
MOVIA	**I**	Move Immediate to ACC	I → ACC	1	-
ADDIA	**I**	Add ACC and Immediate	I + ACC → ACC	1	C, DC, Z
SUBIA	**I**	Subtract ACC from Immediate	I - ACC → ACC	1	C, DC, Z
ANDIA	**I**	AND Immediate with ACC	ACC and I → ACC	1	Z
IORIA	**I**	OR Immediate with ACC	ACC or I → ACC	1	Z
XORIA	**I**	Exclusive OR Immediate to ACC	ACC xor I → ACC	1	Z
RETIA	**I**	Return, place Immediate in ACC	I → ACC, Top of Stack → PC	2	-

Mnemonic, Operands		Description	Operation	Cycles	Status Affected
CALL	I	Call subroutine	PC + 1 → Top of Stack, I → PC<10:0>	2	-
GOTO	I	Unconditional branch	I → PC<10:0>	2	-
BANK	I	Move Immediate to memory bank bits	I → RP<1:0>	1	-

Note:1. 2 cycles for skip, else 1 cycle.
2. bit:Bit address within an 8-bit register R
R:Register address (0x00 to 0x3F)
I:Immediate data
ACC:Accumulator
d:Destination select;
=0 (store result in ACC)
=1 (store result in file register R)
dest:Destination
PC:Program Counter
WDT:Watchdog Timer Counter
GIE:Global interrupt enable bit
$\overline{TO}$:Time-out bit
$\overline{PD}$:Power-down bit
C:Carry bit
DC:Digital carry bit
Z:Zero bit

ADCAR	Add ACC and R with Carry
Syntax:	ADCAR R, d
Operands:	0x00≤R≤0x3F d∈[0,1]
Operation:	R + ACC + C → dest
Status Affected:	C, DC, Z
Description:	Add the contents of the ACC register and register 'R' with Carry. If 'd' is 0 the result is stored in the ACC register. If 'd' is '1' the result is stored back in register 'R'.
Cycles:	1

ADDAR	Add ACC and R
Syntax:	ADDAR R, d
Operands:	0x00≤R≤0x3F d∈[0,1]
Operation:	ACC + R → dest
Status Affected:	C, DC, Z
Description:	Add the contents of the ACC register and register 'R'. If 'd' is 0 the result is stored in the ACC register. If 'd' is '1' the result is stored back in register 'R'.
Cycles:	1

ADDIA	Add ACC and Immediate
Syntax:	ADDIA I
Operands:	0x00≤I≤0xFF
Operation:	ACC + I → ACC
Status Affected:	C, DC, Z
Description:	Add the contents of the ACC register with the 8-bit immediate 'I'. The result is placed in the ACC register.
Cycles:	1

ANDAR	AND ACC and R
Syntax:	ANDAR R, d
Operands:	0x00≤R≤0x3F d∈[0,1]
Operation:	ACC and R → dest
Status Affected:	Z
Description:	The contents of the ACC register are AND'ed with register 'R'. If 'd' is 0 the result is stored in the ACC register. If 'd' is '1' the result is stored back in register 'R'.
Cycles:	1

ANDIA	AND Immediate with ACC
Syntax:	ANDIA I
Operands:	0x00≤I≤0xFF
Operation:	ACC AND I → ACC
Status Affected:	Z
Description:	The contents of the ACC register are AND'ed with the 8-bit immediate 'I'. The result is placed in the ACC register.
Cycles:	1

BANK	Move Immediate to memory bank bits
Syntax:	BANK I
Operands:	0x0≤I≤0x3
Operation:	I → RP<1:0>
Status Affected:	None
Description:	The memory bank bits are loaded with the 2-bit immediate 'I'.
Cycles:	1

BCR	Clear Bit in R
Syntax:	BCR R, b
Operands:	0x00≤R≤0x3F 0x0≤b≤0x7
Operation:	0 → R<b>
Status Affected:	None
Description:	Clear bit 'b' in register 'R'.
Cycles:	1

BSR	Set Bit in R
Syntax:	BSR R, b
Operands:	0x00≤R≤0x3F 0x0≤b≤0x7
Operation:	1 → R<b>
Status Affected:	None
Description:	Set bit 'b' in register 'R'.
Cycles:	1

BTRSC	Test Bit in R, Skip if Clear
Syntax:	BTRSC R, b
Operands:	0x00≤R≤0x3F 0x0≤b≤0x7
Operation:	Skip if R<b> = 0
Status Affected:	None
Description:	If bit 'b' in register 'R' is 0 then the next instruction is skipped. If bit 'b' is 0 then next instruction fetched during the current instruction execution is discarded, and a NOP is executed instead making this a 2-cycle instruction.
Cycles:	1/2

BTRSS	Test Bit in R, Skip if Set
Syntax:	BTRSS R, b
Operands:	0x00≤R≤0x3F 0x0≤b≤0x7
Operation:	Skip if R<b> = 1
Status Affected:	None
Description:	If bit 'b' in register 'R' is '1' then the next instruction is skipped. If bit 'b' is '1', then the next instruction fetched during the current instruction execution, is discarded and a NOP is executed instead, making this a 2-cycle instruction.
Cycles:	1/2

CALL	Subroutine Call
Syntax:	CALL I
Operands:	0x000≤I≤0x3FF
Operation:	PC + 1 → Top of Stack, I → PC<9:0>
Status Affected:	None
Description:	Subroutine call. First, return address (PC+1) is pushed onto the stack. The 10-bit immediate address is loaded into PC bits <9:0>.
Cycles:	2

CLRA	Clear ACC
Syntax:	CLRA
Operands:	None
Operation:	0x00 → ACC; 1 → Z
Status Affected:	Z
Description:	The ACC register is cleared. Zero bit (Z) is set.
Cycles:	1

CLRR	Clear R
Syntax:	CLRR R
Operands:	0x00≤R≤0x3F
Operation:	0x00 → R; 1 → Z
Status Affected:	Z
Description:	The contents of register 'R' are cleared and the Z bit is set.
Cycles:	1

CLRWDT	Clear Watchdog Timer
Syntax:	CLRWDT
Operands:	None
Operation:	0x00 → WDT; 1 → $\overline{TO}$; 1 → $\overline{PD}$
Status Affected:	$\overline{TO}$, $\overline{PD}$
Description:	The CLRWDT instruction resets the WDT. The status bits $\overline{TO}$ and $\overline{PD}$ will be set.
Cycles:	1

COMR	Complement R
Syntax:	COMR R, d
Operands:	0x00≤R≤0x3F d∈[0,1]
Operation:	$\overline{R}$→ dest
Status Affected:	Z
Description:	The contents of register 'R' are complemented. If 'd' is 0 the result is stored in the ACC register. If 'd' is 1 the result is stored back in register 'R'.
Cycles:	1

DECR	Decrement R
Syntax:	DECR R, d
Operands:	0x00≤R≤0x3F d∈[0,1]
Operation:	R - 1 → dest
Status Affected:	Z
Description:	Decrement of register 'R'. If 'd' is 0 the result is stored in the ACC register. If 'd' is 1 the result is stored back in register 'R'.
Cycles:	1

DECRSZ	Decrement R, Skip if 0
Syntax:	DECRSZ R, d
Operands:	0x00≤R≤0x3F d∈[0,1]
Operation:	R - 1 → dest; skip if result =0
Status Affected:	None
Description:	The contents of register 'R' are decrement. If 'd' is 0 the result is placed in the ACC register. If 'd' is 1 the result is stored back in register 'R'. If the result is 0, the next instruction, which is already fetched, is discarded and a NOP is executed instead and making it a 2-cycle instruction.
Cycles:	1/2

GOTO	Unconditional Branch
Syntax:	GOTO I
Operands:	0x000≤I≤0x3FF
Operation:	I → PC<9:0>
Status Affected:	None
Description:	GOTO is an unconditional branch. The 10-bit immediate value is loaded into PC bits <9:0>.
Cycles:	2

INCR	Increment R
Syntax:	INCR R, d
Operands:	0x00≤R≤0x3F d∈[0,1]
Operation:	R + 1 → dest
Status Affected:	Z
Description:	The contents of register 'R' are increment. If 'd' is 0 the result is placed in the ACC register. If 'd' is 1 the result is stored back in register 'R'.
Cycles:	1

INCRSZ	Increment R, Skip if 0
Syntax:	INCRSZ R, d
Operands:	0x00≤R≤0x3F d∈[0,1]
Operation:	R + 1 → dest, skip if result = 0
Status Affected:	None
Description:	The contents of register 'R' are increment. If 'd' is 0 the result is placed in the ACC register. If 'd' is the result is stored back in register 'R'. If the result is 0, then the next instruction, which is already fetched, is discarded and a NOP is executed instead and making it a 2-cycle instruction.
Cycles:	1/2

IORAR	OR ACC with R
Syntax:	IORAR R, d
Operands:	0x00≤R≤0x3F d∈[0,1]
Operation:	ACC or R → dest
Status Affected:	Z
Description:	Inclusive OR the ACC register with register 'R'. If 'd' is 0 the result is placed in the ACC register. If 'd' is 1 the result is placed back in register 'R'.
Cycles:	1

IORIA	OR Immediate with ACC
Syntax:	IORIA I
Operands:	0x00≤I≤0xFF
Operation:	ACC or I → ACC
Status Affected:	Z
Description:	The contents of the ACC register are OR'ed with the 8-bit immediate 'I'. The result is placed in the ACC register.
Cycles:	1

MOVAR	Move ACC to R
Syntax:	MOVAR R
Operands:	0x00≤R≤0x3F
Operation:	ACC → R
Status Affected:	None
Description:	Move data from the ACC register to register 'R'.
Cycles:	1

MOVIA	Move Immediate to ACC
Syntax:	MOVIA I
Operands:	0x00≤I≤0xFF
Operation:	I → ACC
Status Affected:	None
Description:	The 8-bit immediate 'I' is loaded into the ACC register. The don't cares will assemble as 0s.
Cycles:	1

MOVR	Move R
Syntax:	MOVR R, d
Operands:	0x00≤R≤0x3F d∈[0,1]
Operation:	R → dest
Status Affected:	Z
Description:	The contents of register 'R' is moved to destination 'd'. If 'd' is 0, destination is the ACC register. If 'd' is 1, the destination is file register 'R'. 'd' is 1 is useful to test a file register since status flag Z is affected.
Cycles:	1

NOP	No Operation
Syntax:	NOP
Operands:	None
Operation:	No operation
Status Affected:	None
Description:	No operation.
Cycles:	1

RETFIE	Return from Interrupt, Set 'GIE' Bit
Syntax:	RETFIE
Operands:	None
Operation:	Top of Stack → PC 1 → GIE
Status Affected:	None
Description:	The program counter is loaded from the top of the stack (the return address). The 'GIE' bit is set to 1. This is a 2-cycle instruction.
Cycles:	2

RETIA	Return with Immediate in ACC
Syntax:	RETIA I
Operands:	0x00≤I≤0xFF
Operation:	I → ACC; Top of Stack → PC
Status Affected:	None
Description:	The ACC register is loaded with the 8-bit immediate 'I'. The program counter is loaded from the top of the stack (the return address). This is a 2-cycle instruction.
Cycles:	2

RETURN	Return from Subroutine
Syntax:	RETURN
Operands:	None
Operation:	Top of Stack → PC
Status Affected:	None
Description:	The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction.
Cycles:	2

RLR	Rotate Left R through Carry
Syntax:	RLR R, d
Operands:	0x00≤R≤0x3F d∈[0,1]
Operation:	R<7> → C; R<6:0> → dest<7:1>; C → dest<0>
Status Affected:	C
Description:	The contents of register 'R' are rotated left one bit to the left through the Carry Flag. If 'd' is 0 the result is placed in the ACC register. If 'd' is 1 the result is stored back in register 'R'.
Cycles:	1

RRR	Rotate Right R through Carry
Syntax:	RRR R, d
Operands:	0x00≤R≤0x3F d∈[0,1]
Operation:	C → dest<7>; R<7:1> → dest<6:0>; R<0> → C
Status Affected:	C
Description:	The contents of register 'R' are rotated one bit to the right through the Carry Flag. If 'd' is 0 the result is placed in the ACC register. If 'd' is 1 the result is placed back in register 'R'.
Cycles:	1

SLEEP	Enter SLEEP Mode
Syntax:	SLEEP
Operands:	None
Operation:	0x00 → WDT; 1 → $\overline{TO}$; 0 → $\overline{PD}$
Status Affected:	$\overline{TO}$, $\overline{PD}$
Description:	Time-out status bit ($\overline{TO}$) is set. The power-down status bit ($\overline{PD}$) is cleared. The WDT is cleared. The processor is put into SLEEP mode.
Cycles:	1

SBCAR	Subtract ACC from R with Carry
Syntax:	SBCAR R, d
Operands:	0x00≤R≤0x3F d∈[0,1]
Operation:	R + $\overline{ACC}$ + C → dest
Status Affected:	C, DC, Z
Description:	Add the 2's complement data of the ACC register from register 'R' with Carry. If 'd' is 0 the result is stored in the ACC register. If 'd' is 1 the result is stored back in register 'R'.
Cycles:	1

SUBAR	Subtract ACC from R
Syntax:	SUBAR R, d
Operands:	0x00≤R≤0x3F d∈[0,1]
Operation:	R - ACC → dest
Status Affected:	C, DC, Z
Description:	Subtract (2's complement method) the ACC register from register 'R'. If 'd' is 0 the result is stored in the ACC register. If 'd' is 1 the result is stored back in register 'R'.
Cycles:	1

SUBIA	Subtract ACC from Immediate
Syntax:	SUBIA I
Operands:	0x00≤I≤0xFF
Operation:	I - ACC → ACC
Status Affected:	C, DC, Z
Description:	Subtract (2's complement method) the ACC register from the 8-bit immediate 'I'. The result is placed in the ACC register.
Cycles:	1

SWAPR	Swap nibbles in R
Syntax:	SWAPR R, d
Operands:	0x00≤R≤0x3F d∈[0,1]
Operation:	R<3:0> → dest<7:4>; R<7:4> → dest<3:0>
Status Affected:	None
Description:	The upper and lower nibbles of register 'R' are exchanged. If 'd' is 0 the result is placed in ACC register. If 'd' is 1 the result in placed in register 'R'.
Cycles:	1

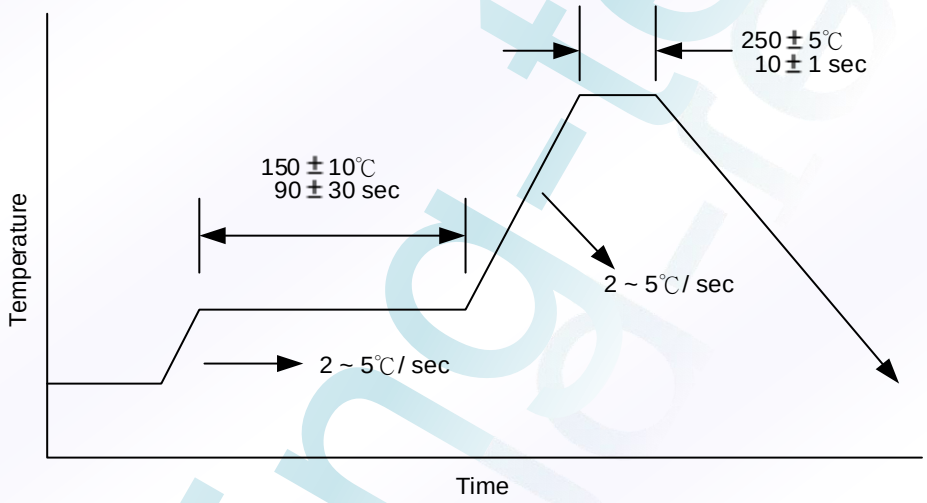
XORAR	Exclusive OR ACC with R
Syntax:	XORAR R, d
Operands:	0x00≤R≤0x3F d∈[0,1]
Operation:	ACC xor R → dest
Status Affected:	Z
Description:	Exclusive OR the contents of the ACC register with register 'R'. If 'd' is 0 the result is stored in the ACC register. If 'd' is 1 the result is stored back in register 'R'.
Cycles:	1

XORIA	Exclusive OR Immediate with ACC
Syntax:	XORIA I
Operands:	0x00≤I≤0xFF
Operation:	ACC xor I → ACC
Status Affected:	Z
Description:	The contents of the ACC register are XOR'ed with the 8-bit immediate 'I'. The result is placed in the ACC register.
Cycles:	1

4.0 ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
	Ambient Operating Temperature	-	0	-	70	°C
	Store Temperature	-	-65	-	150	°C
V_{DD}	DC Supply Voltage	-	0	-	6	V
	Input Voltage with respect to Ground	-	-0.3	-	V_{DD}+0.3	V
	ESD Susceptibility (Standard)	HBM (Human Body Mode)	-	2.0	-	KV
		MM (Machine Mode)	-	200	-	V
	Lead Temperature	Soldering, 10 Sec	-	-	250	°C

4.1 PACKAGE IR Re-flow Soldering Curve



5.0 RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	DC Supply Voltage	-	2.0	-	5.5	V
	Operating Temperature	-	0	-	70	°C

6.0 ELECTRICAL CHARACTERISTICS

6.1 AC Characteristics

Ta=25°C

Symbol	Description	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
F_{HIRC}	High Frequency IRC	Low	V_{DD}=3V	-3%	8	+3%	M_{HZ}
		High	V_{DD}=5V				
F_{LIRC}	Low Frequency IRC	3V	-	-	43.74	-	K_{HZ}
		5V		-	60.78	-	
T_{WDT}	WDT period time	3V	WDT=18mS	-	23.45	-	mS
		5V		-	16.8	-	
		3V	WDT=72mS	-	93.88	-	
		5V		-	67.2	-	
		3V	WDT=288mS	-	381	-	
		5V		-	272	-	
		3V	WDT=2Sec	-	3.05	-	S
		5V		-	2.17	-	

Note: 1. At any time, a 0.1μF decoupling capacitor should be connected between V_{DD} and V_{SS} and device as close as possible.

2. LIRC 55K_{HZ} is an uncalibrated low-frequency oscillator, frequency is for reference only.

6.2 DC Characteristics

Ta=25°C

Symbol	Description	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{IH}	Input high voltage, I/O Ports (Without IOB3 Pin)	3V	-	-	1.26	V_{DD}	V
		5V		-	1.78		
	Input high voltage, IBO3 Pin	3V	-	-	1.25	V_{DD}	
		5V		-	1.9		
V_{IL}	Input low voltage, I/O Ports (Without IOB3 Pin)	3V	-	V_{SS}	0.99	-	V
		5V			1.24	-	
	Input low voltage, IOB3 Pin	3V	-	V_{SS}	0.92	-	
		5V			1.15	-	
V_{LVDT}	Low voltage detect	-	LVDT=3.6V	-	3.6	-	V
		-	LVDT=2.6	-	2.6	-	
		-	LVDT=2.4V	-	2.4	-	
		-	LVDT=2.2V	-	2.2	-	
		-	LVDT=2.0V	-	2.0	-	
		-	LVDT=1.8V	-	1.8	-	
I_{OH}	I/O Ports Drive current (Without IOB3 Pin)	3V	V_{OH}=0.9V_{DD}	-	1.61	-	mA
		5V		1.5	4.12	-	
I_{OL}	I/O Ports Sink current (Without IOB3 Pin)	3V	V_{OL}=0.1V_{DD}	-	9.51	-	mA
		5V		15	22.69	-	
	IOB3 Pin Sink current	3V	V_{OL}=0.1V_{DD}	-	10.55	-	
		5V		-	25.59	-	
I_{PH}	I/O Ports Pull-high current	3V	Input pin at V_{SS}	-	20.55	-	uA
		5V		55	68.51	85	

Symbol	Description	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
I_{LVDT}	LVDT current	5V	LVDT3.6	-	1.13	-	uA
		3V	LVDT2.6	-	0.43	-	
		5V		-	1.46	-	
		3V	LVDT2.4	-	0.46	-	
		5V		-	1.57	-	
		3V	LVDT2.2	-	0.49	-	
		5V		-	1.7	-	
I_{LVDT}	LVDT current	3V	LVDT2.0	-	0.53	-	uA
		5V		-	1.83	-	
		3V	LVDT1.8	-	0.6	-	
		5V		-	2.05	-	
I_{WDT}	WDT current	3V	Sleep mode, 2Sec	-	0.47	-	uA
		5V		-	2.68	-	
I_{SB}	Sleep mode (Power down) current	3V	-	-	<1	-	uA
		5V		-	<1	1	
I_{DD}	Operating current	3V	F_{CPU} = 8M$_{HZ}$ (4MIPS)	-	0.64	-	mA
		5V		-	1.28	-	

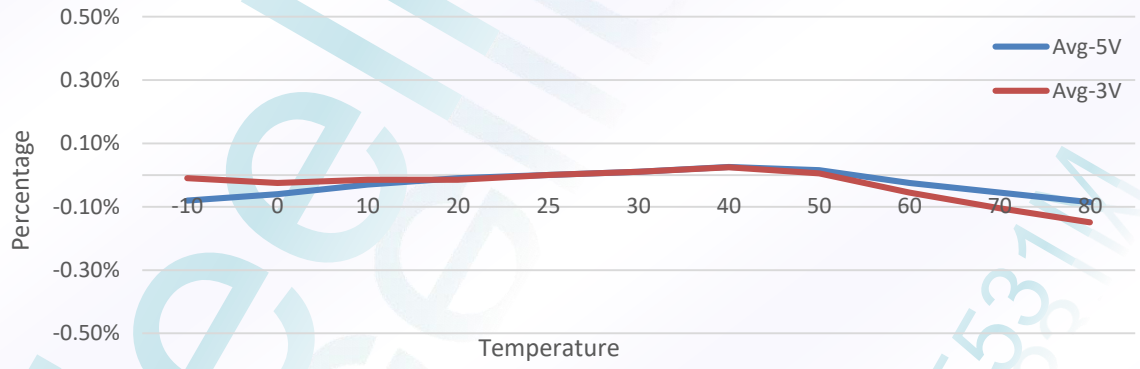
6.3 Comparator Characteristics

Ta=25°C

Symbol	Description	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{IO}	Comparator input offset voltage	-	-	-	-	-	mV
V_{ICM}	Comparator input common mode voltage	-	-	0	-	V_{DD}	V

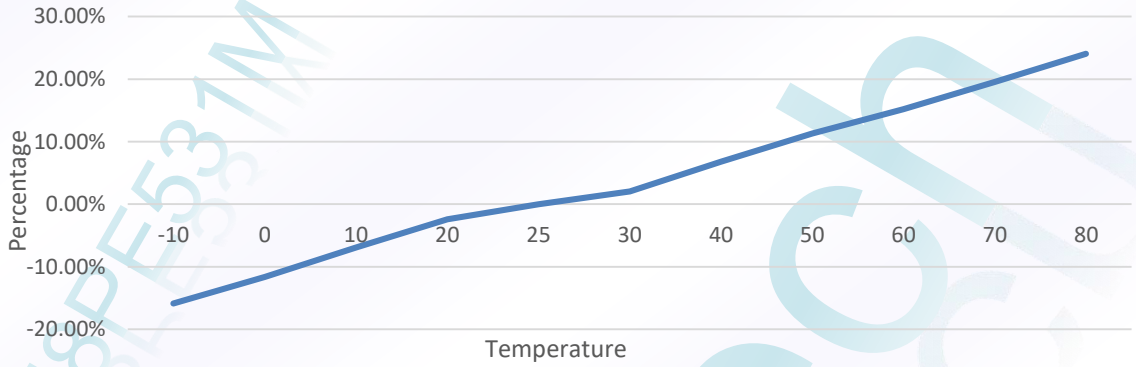
6.4 ELECTRICAL CHARACTERISTICS Typical charts of FM8PE531M

6.4.1 HIRC 8M$_{HZ}$ vs. Temperature



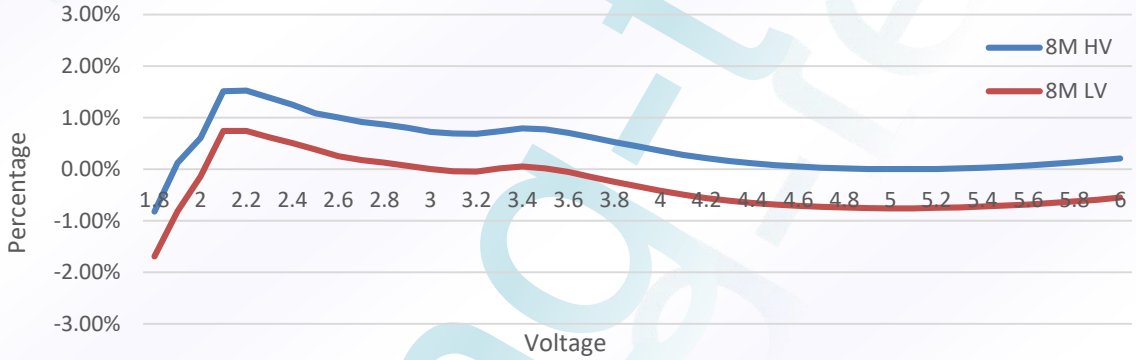
Note: Curves are for design reference only.

6.4.2 LIRC 55K$_{HZ}$ vs. Temperature



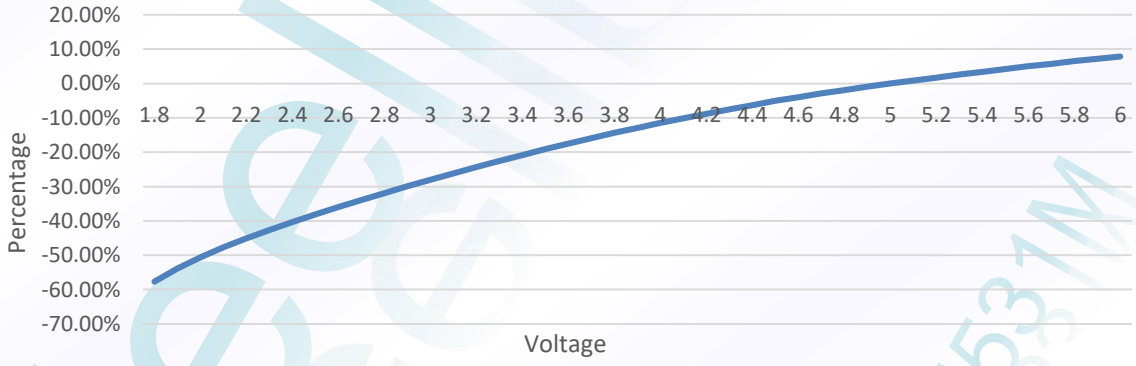
Note: Curves are for design reference only.

6.4.3 HIRC 8 M$_{HZ}$ vs. Supply Voltage (Ta=25°C)



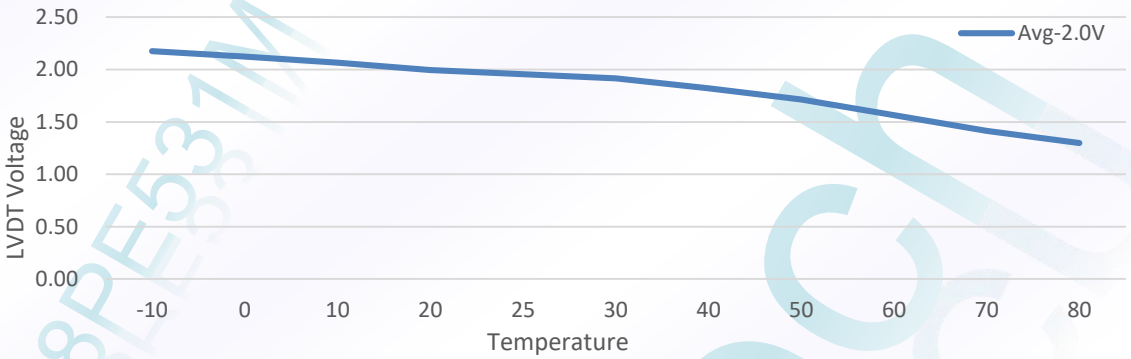
Note: Curves are for design reference only.

6.4.4 LIRC 55K$_{HZ}$ vs. Supply Voltage (Ta=25°C)



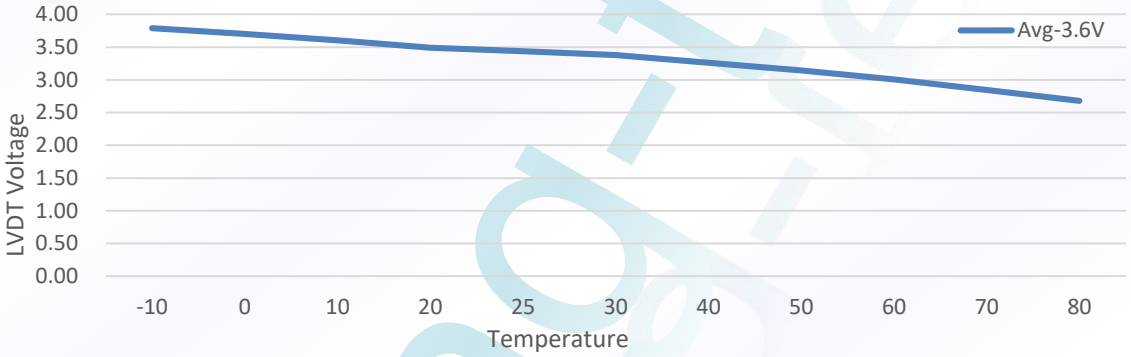
Note: Curves are for design reference only.

6.4.5 Low Voltage Detect (LVDT=2.0V) vs. Temperature



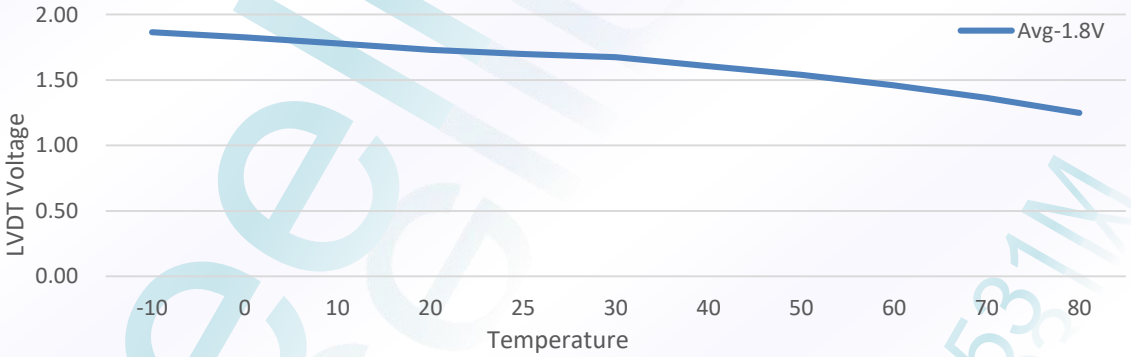
Note: Curves are for design reference only.

6.4.6 Low Voltage Detect (LVDT=3.6V) vs. Temperature



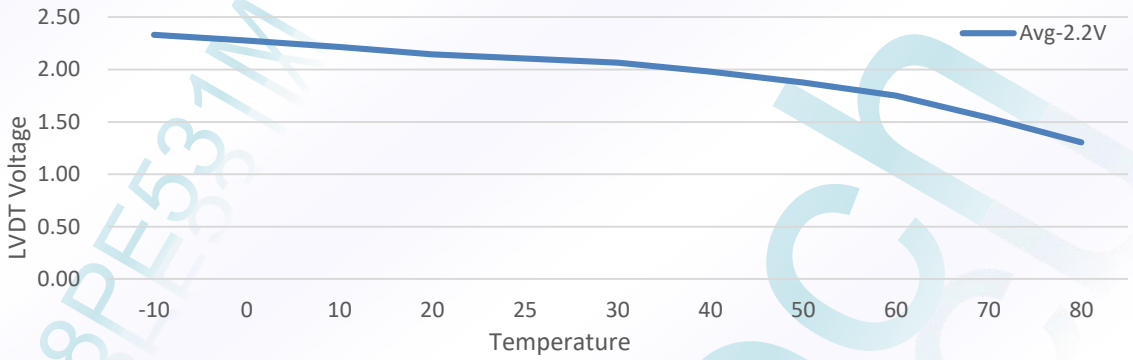
Note: Curves are for design reference only.

6.4.7 Low Voltage Detect (LVDT=1.8V) vs. Temperature



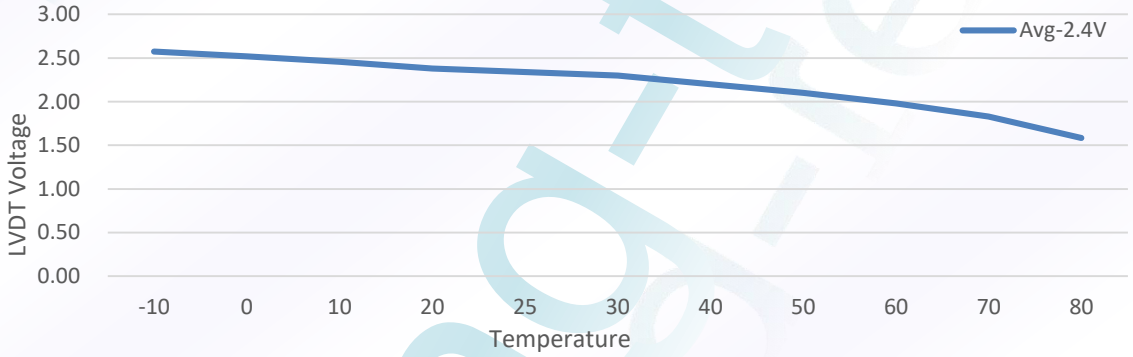
Note: Curves are for design reference only.

6.4.8 Low Voltage Detect (LVDT=2.2V) vs. Temperature



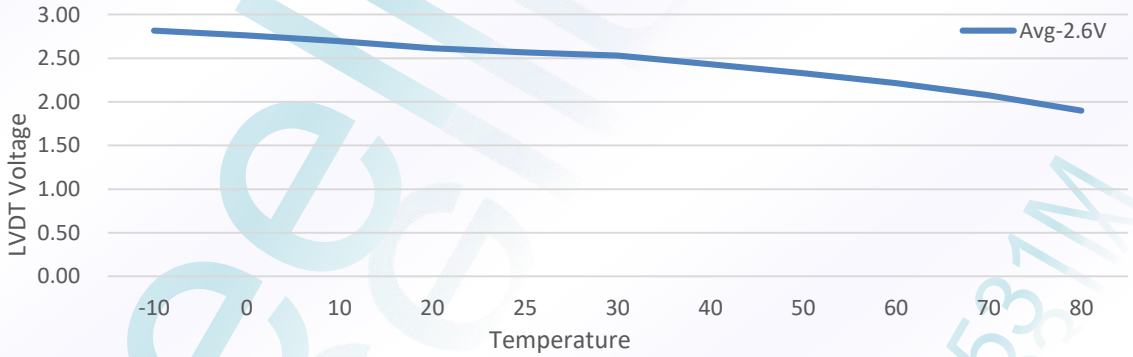
Note: Curves are for design reference only.

6.4.9 Low Voltage Detect (LVDT=2.4V) vs. Temperature



Note: Curves are for design reference only.

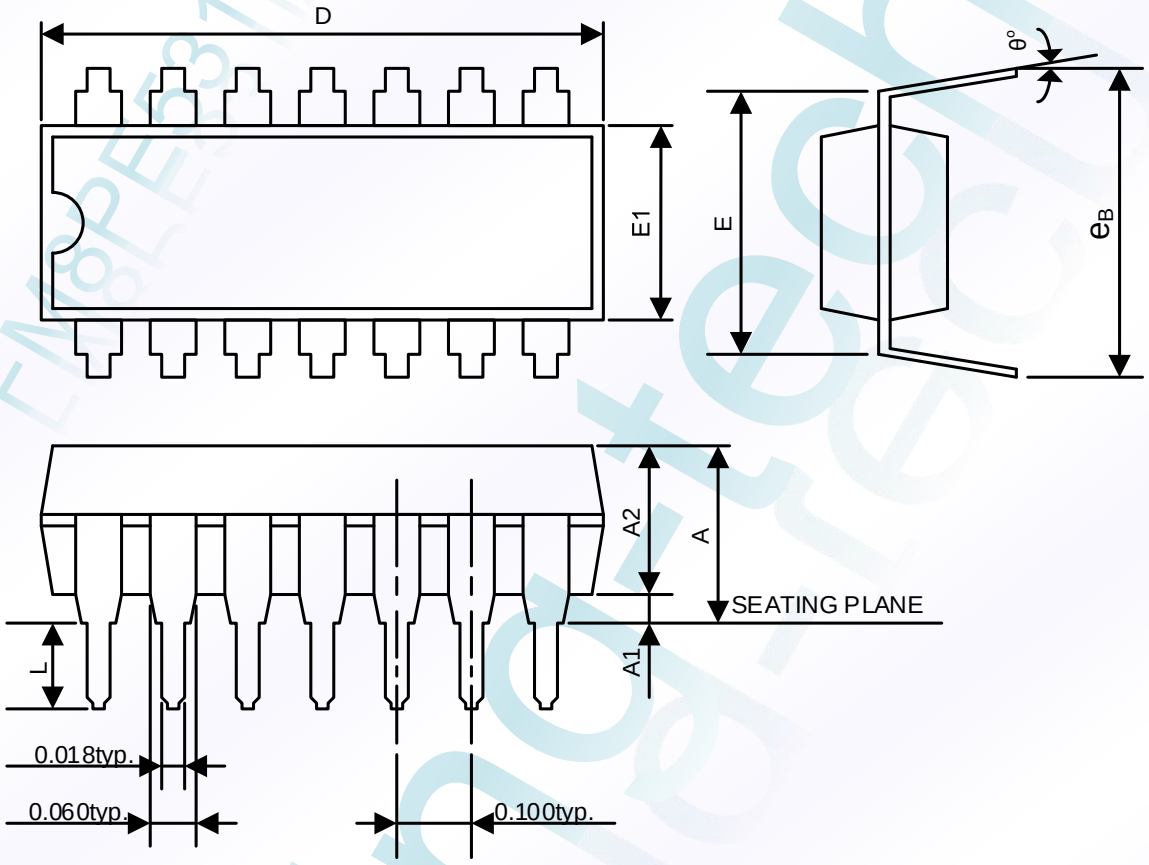
6.4.10 Low Voltage Detect (LVDT=2.6V) vs. Temperature



Note: Curves are for design reference only.

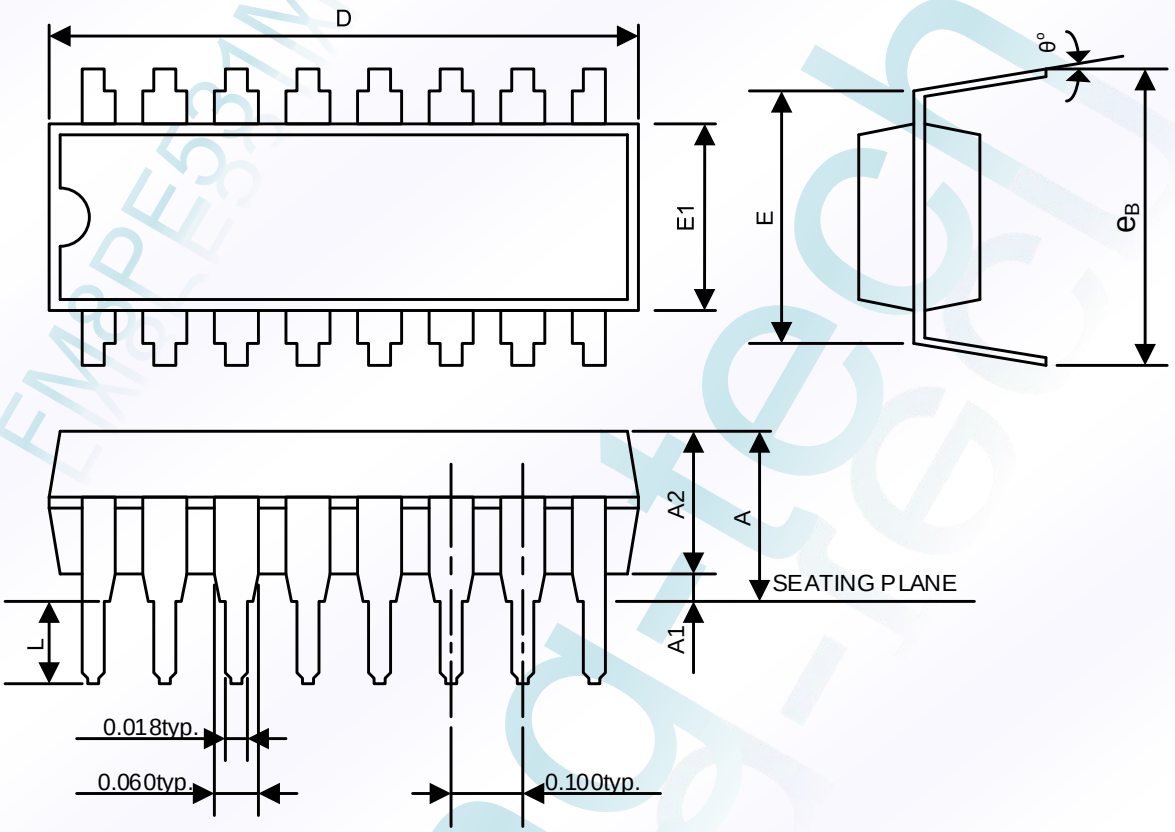
7.0 PACKAGE DIMENSION

7.1 14-PIN PDIP



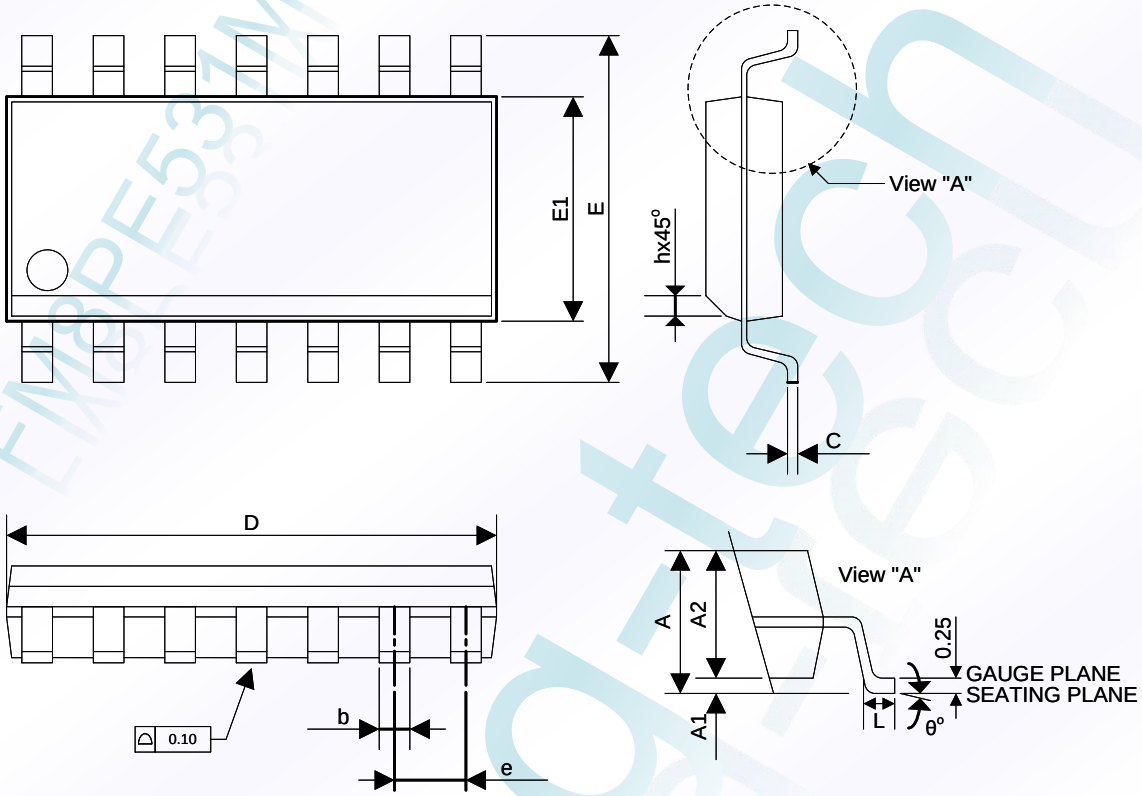
Symbols	Dimension In Inches		
	Min	Nom	Max
A	-	-	0.210
A1	0.015	-	-
A2	0.125	0.130	0.135
D	0.735	0.750	0.775
E		0.300 BSC.	
E1	0.245	0.250	0.255
L	0.115	0.130	0.150
eB	0.335	0.355	0.375
θ°	0°	7°	15°

7.2 16-PIN PDIP



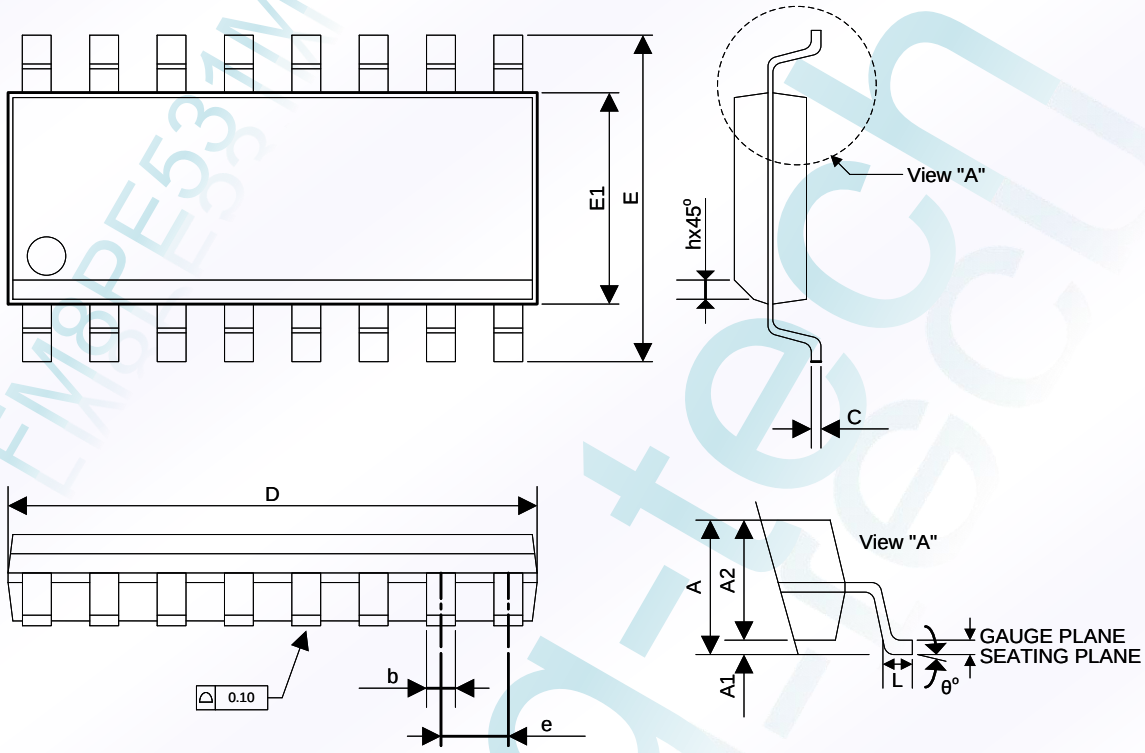
Symbols	Dimension In Inches		
	Min	Nom	Max
A	-	-	0.172
A1	0.015	-	0.038
A2	0.125	0.130	0.135
D	0.735	0.755	0.775
E		0.300 BSC.	
E1	0.245	0.250	0.255
L	0.115	0.130	0.150
eB	0.335	0.355	0.375
θ°	0°	7°	15°

7.3 14-PIN SOP 150mil



Symbols	Dimension In MM		
	Min	Nom	Max
A	-	-	1.75
A1	0.10	-	0.25
A2	1.25	-	-
b	0.31	-	0.51
C	0.10	-	0.25
D	8.65 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
L	0.40	-	1.27
H	0.25		0.50
θ	0°	-	8°

7.4 16-PIN SOP 150mil



Symbols	Dimension In MM		
	Min	Nom	Max
A	-	-	1.75
A1	0.10	-	0.25
A2	1.25	-	-
b	0.31	-	0.51
c	0.10	-	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
L	0.40	-	1.27
H	0.25	-	0.50
θ	0°	-	8°

8.0 ORDERING INFORMATION

OTP Type MCU	Package Type	Pin Count	Package Size	MOQ	MSL	Sample Stock
FM8PE531MAP	PDIP	14	300mil	3,000EA/Tube	3	Available
FM8PE531MAP	SOP	14	300mil	3,000EA/Tube 3,000EA/Reel	3	Available
FM8PE531MBP	PDIP	16	300mil	3,000EA/Tube	3	Available
FM8PE531MBD	SOP	16	150mil	3,000EA/Tube 3,000EA/Reel	3	Available